Secondary-Side Synchronous Forward Controller

FEATURES

- **Secondary-Side Control for Fast Transient Response**
- **Self-Starting Architecture Eliminates Need for Separate Bias Regulator**
- **Proprietary Gate Drive Encoding Scheme Reduces System Complexity**
- Current Mode Control Ensures Current Sharing
- PLL Fixed Frequency: 100kHz to 500kHz
- ±1% Output Voltage Accuracy
- OPTI-LOOP Compensation
- Available in a Narrow 16-Lead SSOP Package

APPLICATIONS

- Isolated 48V Telecommunication Systems
- Internet Servers and Routers
- Distributed Power Step-Down Converters
- Automotive and Heavy Equipment

DESCRIPTION

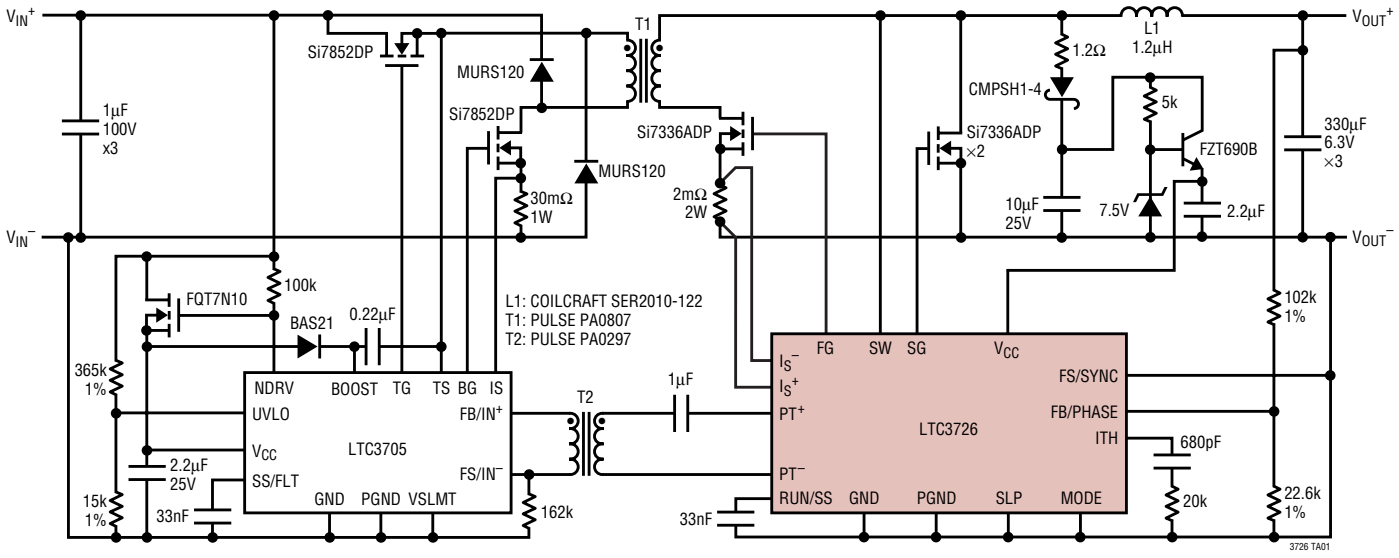
The LTC®3726 is a secondary-side controller for synchronous forward converters. When used in conjunction with the LTC3705/LTC3725 gate driver and primary-side controllers, the part creates a complete isolated power supply that combines the simplicity of OPTI-LOOP® compensation with the speed of secondary-side control.

The LTC3726 has been designed to simplify the design of highly efficient, secondary-side forward converters. Working in concert with the LTC3705 or LTC 3725, the LTC3726 forms a robust, self-starting converter that eliminates the need for the separate bias regulator that is commonly used in secondary-side control applications. In addition, a proprietary scheme is used to multiplex gate drive signals and DC bias power across the isolation barrier through a single, tiny pulse transformer.

The LTC3726 is available in a 16-lead SSOP package.

TYPICAL APPLICATION

36V-72V to 3.3V/20A Isolated Forward Converter

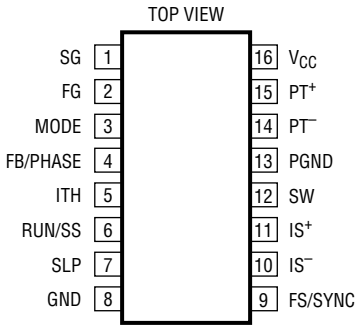


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} ..... –0.3V to 10V
SW ..... –5V to 50V
ITH, RUN/SS ..... –0.3V to 7V
All Other Pins ..... –0.3V to 10V
Operating Ambient Temperature Range (Note 2)
LTC3726EGN ..... –40°C to 85°C
LTC3726IGN ..... –40°C to 85°C
Operating Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC3726EGN
LTC3726IGN

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 7V, GND = PGND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{FB}	Regulated Feedback Voltage	(Note 4) ITH = 1.2V	●	0.594	0.600	0.606	V
$\Delta V_{FB(LINREG)}$	Feedback Voltage Line Regulation	V_{CC} = 5V to 10V, ITH = 1.2V			0.001		%/V
$\Delta V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	Measured in Servo Loop, ITH = 0.5V to 2V	●		–0.01	–0.1	%
V_{ISMAX}	Maximum Current Sense Threshold	R_{SENSE} Mode, V_{IS} = 0V CT Mode, V_{IS} = 0V		68 1.15	78 1.28	88 1.4	mV V
V_{ISOC}	Over-Current Shutdown Threshold	R_{SENSE} Mode, V_{IS} = 0V CT Mode, V_{IS} = 0V		87 1.45	100 1.65	113 1.85	mV V
g_m	Transconductance Amplifier g_m			2.40	2.75	3.10	mS
$I_{RUN/SS(C)}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 2V		–4	–5	–6	µA
$I_{RUN/SS(D)}$	Soft-Start Discharge Current				3		µA
$V_{RUN/SS}$	RUN/SS Pin ON Threshold	$V_{RUN/SS}$ Rising	●	0.4	0.45	0.5	V
$t_{ON,MIN}$	Minimum ON Time				200		ns
FG, SG R_{UP}	FG, SG Driver Pull-Up On Resistance	FG, SG Low			1.5	2.3	Ω
FG, SG R_{DOWN}	FG, SG Driver Pull-Down On Resistance	FG, SG High			1.5	2.3	Ω
PT^+, PT^- R_{UP}	PT^+, PT^- Driver Pull-Up Resistance	PT^+, PT^- Low			1.5	2.3	Ω
PR^+, PT^- R_{DOWN}	PT^+, PT^- Driver Pull-Down Resistance	PT^+, PT^- High			1.5	2.3	Ω
$\Delta V_{FB(OV)}$	Output Overvoltage Threshold	V_{FB} Rising		15	17	19	%

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 7V, GND = PGND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Supply							
V_{CCOP}	Operating Voltage Range			5		10	V
I_{CC}	Supply Current Operating Shutdown	 f_{OSC} = 200kHz (Note 5) $V_{RUN/SS}$ = GND			 4.2 700		 mA µA
V_{UVLO}	UV Lockout	V_{CC} Rising	●	4.52	4.60	4.70	V
V_{HYS}	UV Hysteresis				0.4		V
Oscillator and Phase-Locked Loop							
I_{FS}	FS/SYNC Pin Sourcing Current				20		µA
f_{LOW}	Oscillator Low Frequency Set Point	$V_{FS/SYNC}$ = GND		170	200	230	kHz
f_{HIGH}	Oscillator High Frequency Set Point	$V_{FS/SYNC}$ = V_{CC}		255	300	345	kHz
Δf (R_{FS})	Oscillator Resistor Set Accuracy	75kΩ < $R_{FS/SYNC}$ < 175kΩ		–20		20	%
$f_{PLL(MAX)}$	Maximum PLL Sync Frequency				500		kHz
$f_{PLL(MIN)}$	Minimum PLL Sync Frequency				75		kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3726E is guaranteed to meet the performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3726I is guaranteed and tested over the full –40°C to 85°C operating temperature range.

Note 3: Operating junction temperature T_J (in °C) is calculated from the ambient temperature T_A and the average power dissipation P_D (in Watts) by the formula:

$$T_J = T_A + \theta_{JA} \bullet P_D$$

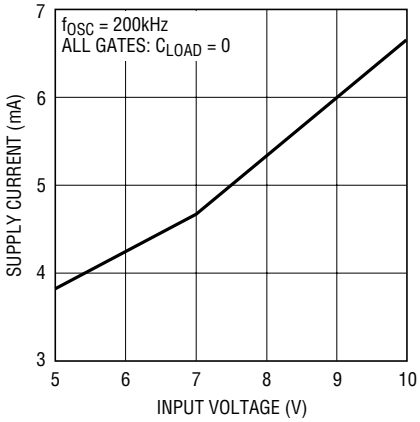
Refer to the Applications Information section for details.

Note 4: The LTC3726 is tested in a feedback loop that servos V_{FB} to a voltage near the internal 0.6V reference voltage to obtain the specified ITH voltage (V_{ITH} = 1.2V).

Note 5: Operating supply current is measured in test mode. Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency. See Typical Performance Characteristics.

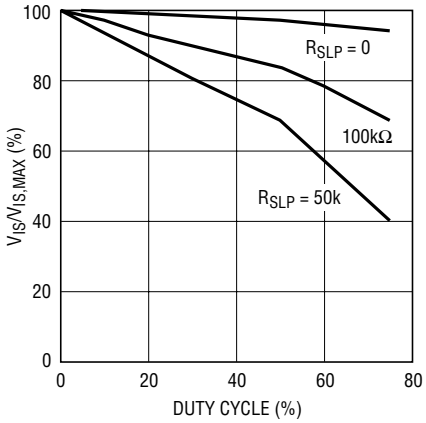
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

V_{CC} Supply Current vs Input Voltage



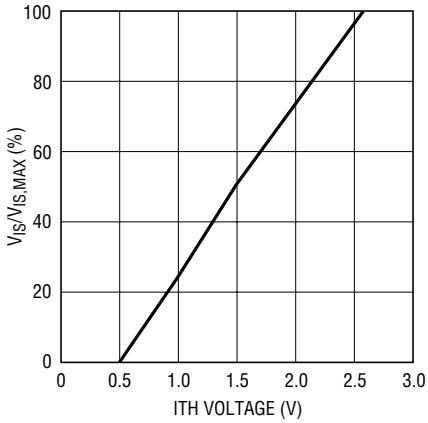
3726 G01

Maximum Current Sense Threshold vs Duty Cycle



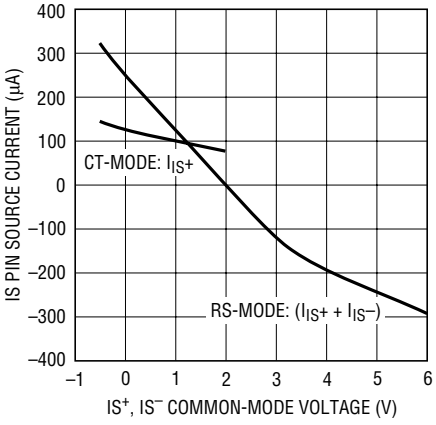
3726 G03

Maximum Current Sense Threshold vs ITH Voltage



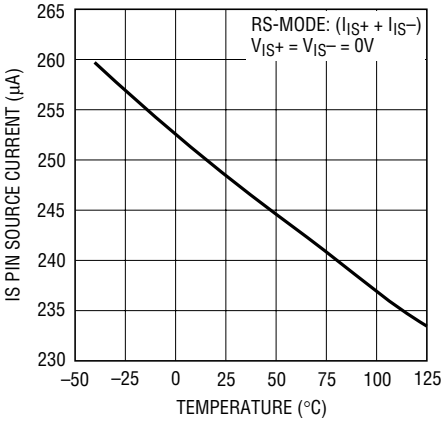
3726 G04

IS Pins Source Current



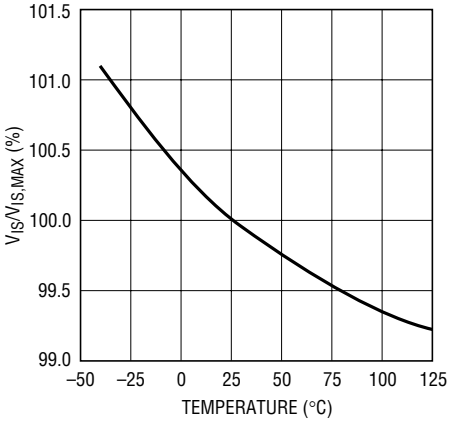
3726 G05

IS Pins Source Current vs Temperature



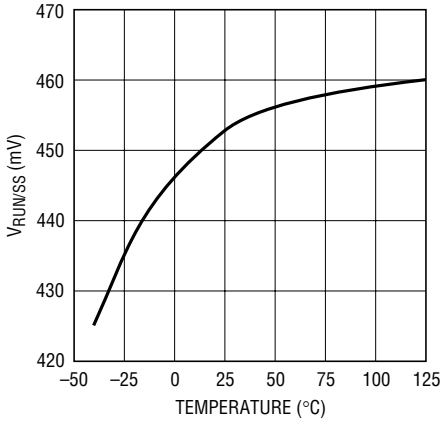
3726 G06

Maximum Current Sense Threshold vs Temperature



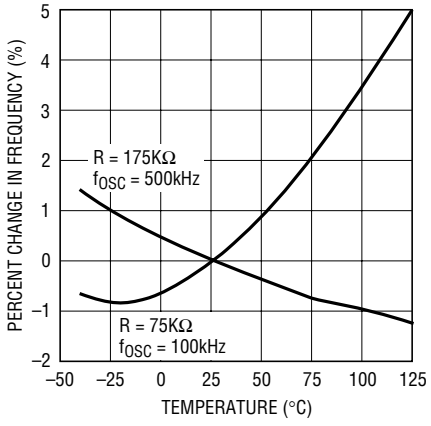
3726 G07

RUN/SS ON Threshold vs Temperature



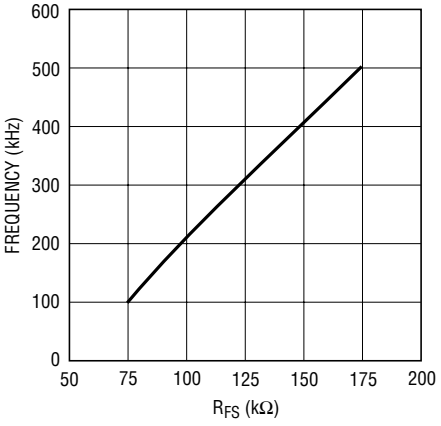
3726 G08

Oscillator Frequency vs Temperature



3726 G14

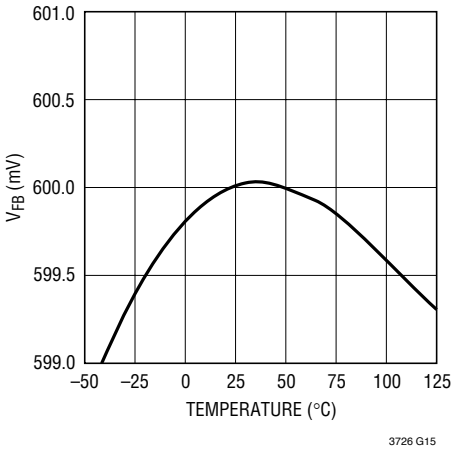
Oscillator Frequency vs R_{FS}



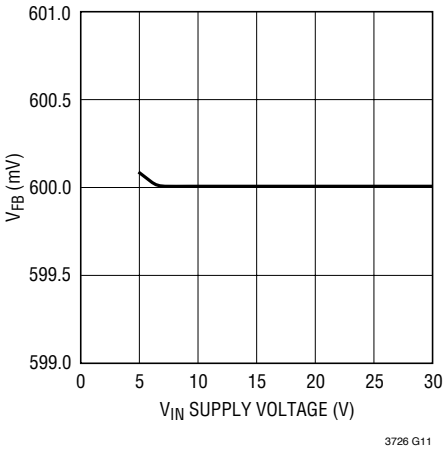
3726 G09

TYPICAL PERFORMANCE CHARACTERISTICS

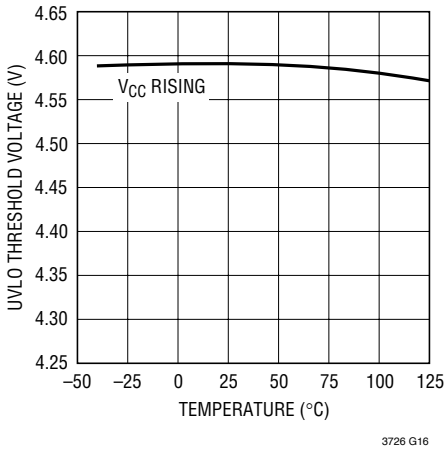
FB Voltage vs Temperature



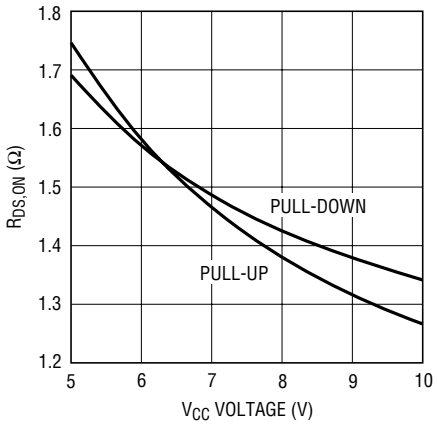
FB Voltage Line Regulation



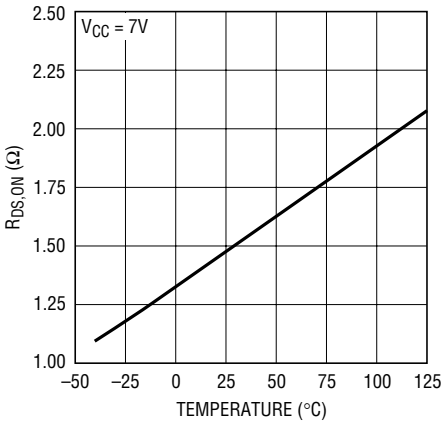
Undervoltage Lockout vs Temperature



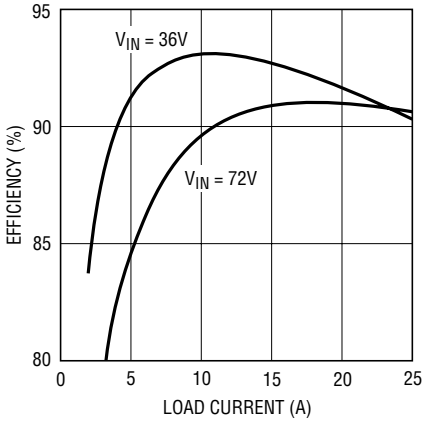
Gate Driver On-Resistance vs V_{CC}



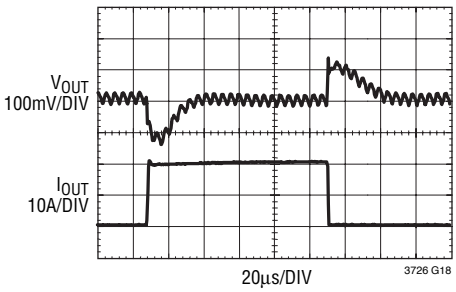
Gate Driver On-Resistance vs Temperature



Efficiency (Figure 5)



Load Step (Figure 5)



V_{IN} = 48V
V_{OUT} = 3.3V
LOAD STEP = 0A TO 20A

PIN FUNCTIONS

SG (Pin 1): Gate Drive for the "Synchronous" MOSFET.

FG (Pin 2): Gate Drive for the "Forward" MOSFET.

MODE (Pin 3): Tie to either GND or V_{CC} to set the maximum duty cycle at either 50% or 75% respectively. Tie to ground through either a 200k or 100k resistor (50% or 75% maximum duty cycle) to disable pulse encoding. In this mode, normal PWM signals will be generated at the PT^+ pin, while a clock signal is generated at the PT^- pin.

FB/PHASE (Pin 4): Inverting input of the main loop Error Amplifier and Control Input to the Phase Selector. In PolyPhase® Slave applications (where voltage feedback is not needed) this pin is used to determine the phasing of the controller CLK relative to the synchronizing signal at the FS/SYNC pin.

ITH (Pin 5): The Output of the Main Loop Error Amplifier. Place compensation components between the ITH pin and GND.

RUN/SS (Pin 6): Combination Run Control and Soft-Start Inputs. A capacitor to ground sets the ramp time of the output voltage. Holding this pin below 0.4V causes the IC to shut down all internal circuitry.

SLP (Pin 7): Slope Compensation Input. Place a single resistor to ground to set the desired amount of slope compensation.

GND (Pin 8): Signal Ground.

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FS/SYNC (Pin 9): Combination Frequency Set and SYNC pin. Tie to GND or V_{CC} to run at 200kHz and 300kHz respec-tively. Place a single resistor to ground at this pin to set the frequency between 75kHz and 500kHz. To synchronize, drive this pin with a clock signal to achieve PLL synchronization from 75kHz to 500kHz. Sources 20μA of current.

I_S^- (Pin 10): Negative Input to the Current Sense Circuit. When using current sense transformers, this pin may be tied to V_{CC} for single-ended sensing with a 1.28V maximum current trip level.

I_S^+ (Pin 11): Positive Input to the Current Sense Circuit. Connect to the positive end of a current sense resistor or to the output of a current sense transformer.

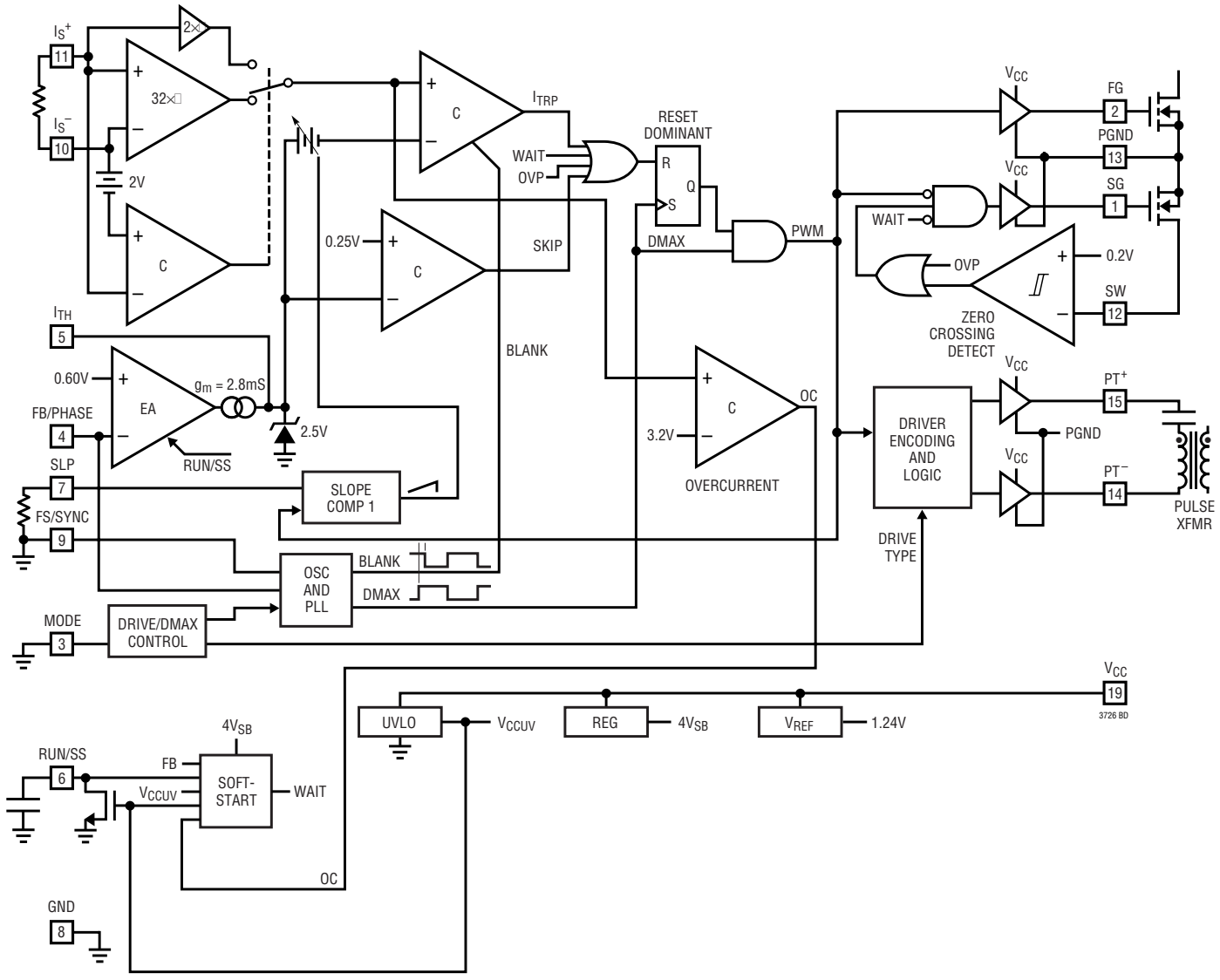
SW (Pin 12): Connect to the drain of the "synchronous" MOSFET. This input is used for adaptive shoot-through prevention and leading edge blanking.

PGND (Pin 13): Gate Driver Ground Pin.

PT^-, PT^+ (Pins 14, 15): Pulse Transformer Driver Outputs. For most applications, these connect to a pulse transformer (with a series DC blocking capacitor). The PWM information is multiplexed together with DC power and sent through a single pulse transformer to the primary side. This information may be decoded by the LTC3705 gate driver and primary-side controller.

V_{CC} (Pin 16): Main V_{CC} Input for all Driver and Control Circuitry.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3726 is designed to work in a constant frequency, current mode, one or two transistor forward converter. During normal operation, the primary-side MOSFET(s) is (are) "clocked" on with the forward MOSFET on the secondary side. This applies the reflected input voltage across the inductor on the secondary side. When the current in the inductor has ramped up to the peak value as commanded by the voltage on the ITH pin, the current sense comparator is tripped, turning off the primary-side and forward MOSFETs. To avoid turning on the synchronous MOSFET prematurely and causing shoot-through, the voltage on the SW pin is monitored. This voltage will usually fall below 0V soon after the primary-side MOSFETs have turned completely off. When this condition is detected, the synchronous MOSFET is quickly turned on, causing the inductor current to ramp back downwards. The error amplifier senses the output voltage, and adjusts the ITH voltage to obtain the peak current needed to maintain the desired main-loop output voltage. The LTC3726 always operates in a continuous current, synchronous switching mode. This ensures a rapid transient response as well as a stable bias supply voltage at light loads. A maximum duty cycle (either 50% or 75%) is internally set via clock dividers to prevent saturation of the main transformer. In the event of an overvoltage on the output, the synchronous MOSFET is quickly turned on to help protect critical loads from damage.

Gate Drive Encoding

Since the LTC3726 controller resides on the secondary side of an isolation barrier, communication to the primary-side power MOSFETs is generally done through a transformer. Moreover, it is often necessary to generate a low voltage bias supply for the primary-side gate drive circuitry. In order to reduce the number of isolated windings present in the system, the LTC3726 uses a proprietary scheme to encode the PWM gate drive information and multiplex it together with bias power for the primary-side drive and control, using a single pulse transformer. Note that, unlike optoisolators and other modulation techniques, this multiplexing scheme does not introduce a significant time delay into the system.

For most forward converter applications, the PT^+ and PT^- outputs will contain a pulse-encoded PWM signal. These outputs are driven in a complementary fashion with an essentially constant 50% duty cycle. This results in a stable volt-second balance as well as an efficient transfer of bias power across the pulse transformer. As shown in Figure 1, the beginning of the positive half-cycle coincides with the turn-on of the primary-side MOSFET(s). Likewise, the beginning of the negative half-cycle coincides with the maximum duty cycle (forced turn-off of primary switch(es)). At the appropriate time during the positive half-cycle, the end of the "on" time (PWM going LOW) is signaled by briefly applying a zero volt differential across the pulse transformer. Figure 1 illustrates the operation of this multiplexing scheme.

The LTC3705 primary-side controller and gate driver will decode this PWM information as well as extract the power needed for primary-side gate drive.

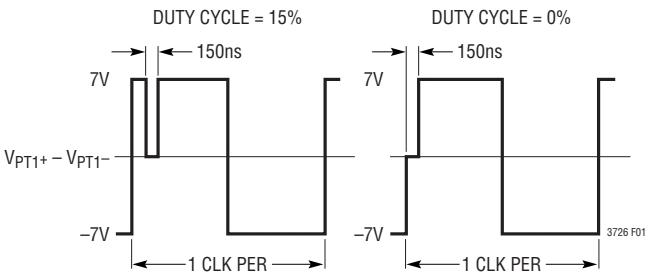


Figure 1: Gate Drive Encoding Scheme (V_{MODE} = GND)

Self-Starting Architecture

When the LTC3726 is used in conjunction with the LTC3705/LTC3725 primary-side controller and gate driver, a complete self-starting isolated supply is formed. When input voltage is first applied in such an application, the LTC3705/LTC3725 will begin switching in an "open-loop" fashion, causing the main output to slowly ramp upwards. This is the primary-side soft-start mode. On the secondary side, the LTC3726 derives its operating bias voltage from a peak-charged capacitor. This peak-charged voltage will rise more rapidly than the main output of the converter, so that the LTC3726 will become operational well before the output voltage has reached its final value.

OPERATION

When the LTC3726 has adequate operating voltage, it will begin the procedure of assuming control from the primary side. To do this, it first measures the voltage on the power supply's main output and then automatically advances its own soft-start voltage to correspond to the main output voltage. This ensures that the output voltage increases monotonically as the soft-start control is transferred from primary to secondary. The LTC3726 then begins sending PWM signals to the LTC3705/LTC3725 on the primary side through a pulse transformer. When the LTC3705/LTC3725 has detected a stable signal from the secondary controller, it transfers control of the primary switches over to the LTC3726, beginning the secondary-side soft-start mode. The LTC3726 continues in this mode until the output voltage has ramped up to its final value. If for any reason, the LTC3726 either stops sending (or initially fails to send) PWM information to the LTC3705/LTC3725, the LTC3705/LTC3725 will detect a FAULT and initiate a soft-start retry (see the LTC3705/LTC3725 data sheet).

Slope Compensation

Slope compensation is added at the input of the PWM comparator to improve stability and noise margin of the peak current control loop. The amount of slope compensation can be selected from one of five preprogrammed values using the SLP pin as shown in Table 1. Note that the amount of slope compensation doubles when the duty cycle exceeds 50%.

Table 1

SLP PIN	SLOPE (D < 0.5)	SLOPE (D > 0.5)
GND	$0.05 \bullet I_{SMAX} \bullet f_{OSC}$	$0.1 \bullet I_{SMAX} \bullet f_{OSC}$
V_{CC}	None	None
400kΩ to GND	$0.1 \bullet I_{SMAX} \bullet f_{OSC}$	$0.2 \bullet I_{SMAX} \bullet f_{OSC}$
200kΩ to GND	$0.15 \bullet I_{SMAX} \bullet f_{OSC}$	$0.3 \bullet I_{SMAX} \bullet f_{OSC}$
100kΩ to GND	$0.25 \bullet I_{SMAX} \bullet f_{OSC}$	$0.5 \bullet I_{SMAX} \bullet f_{OSC}$
50kΩ to GND	$0.5 \bullet I_{SMAX} \bullet f_{OSC}$	$1.0 \bullet I_{SMAX} \bullet f_{OSC}$

In Table 1 above, I_{SMAX} is the maximum current limit, and f_{OSC} is the switching frequency.

Current Sensing and Current Limit

For current sensing, the LTC3726 supports either a current sense resistor or a current sense transformer. The current sense resistor may either be placed in series with the inductor (either high side or ground lead sensing), or in the source of the "forward" switch. If a current sense transformer is used, the I_S^- input should be tied to V_{CC} and the I_S^+ pin to the output of the current sense transformer. This causes the gain of the internal current sense amplifier to be reduced by a factor of 16, so that the maximum current sense voltage (current limit) is increased from 78mV to 1.28V. An internal, adaptive leading edge blanking circuit ensures clean operation for "switch" current sensing applications.

Current limit is achieved in the LTC3726 by limiting the maximum voltage excursion of the error signal (I_{TH} voltage). Note that if slope compensation is used, the precise value at which current limit occurs will be a function of duty cycle (see Typical Performance Characteristics). If a short circuit is applied, an independent overcurrent comparator may be tripped. In this case, the LTC3726 will enter a "hiccup" mode using the soft-start circuitry.

Frequency Setting and Synchronization

The LTC3726 uses a single pin to set the operating frequency, or to synchronize the internal oscillator to a reference clock with an on-chip phase-locked loop (PLL). The FS pin may be tied to GND, V_{CC} or have a single resistor to GND to set the switching frequency. If a clock signal (>2V) is detected at the FS pin, the LTC3726 will automatically synchronize to the rising edge of the reference clock. Table 2 summarizes the operation of the FS pin.

For synchronization between multiple LTC3726s, the PT^+ pin of one LTC3726 can be used as a master clock reference and tied to the FS pin of the other LTC3726s.

Table 2

FS PIN	SWITCHING FREQUENCY
GND	200kHz
V_{CC}	300kHz
R_{FS} to GND	f_{OSC} (Hz) = $4R_{FS}$ – 200k
Reference Clock	$f_{OSC} = f_{REF}$ (75kHz to 500kHz)

This will cause all LTC3726s to operate at the same frequency and phase. The LTC3726 can also be used as a "Slave" in a PolyPhase application. In this case, the phase angle of each LTC3726 can be set by using the FB/PHASE

OPERATION

pin (see Slave Mode Operation). The Phase angle cannot be adjusted when the FB/PHASE pin is being used for voltage loop regulation.

Soft-Start

The soft-start circuitry has four functions: 1) to provide a shutdown, 2) to provide a smooth ramp on the output voltage during start-up, 3) to limit the output current in a short-circuit situation by entering a hiccup mode, and 4) to communicate fault and shutdown information between multiple LTC3726s in a PolyPhase application.

When the RUN/SS pin is pulled to GND, the chip is placed into shutdown mode. If this pin is released, the RUN/SS pin is initially charged with a 50μA current source. After the RUN/SS pin gets above 0.5V, the chip is enabled. At the instant that the LTC3726 is first enabled, the RUN/SS voltage is rapidly preset to a voltage that will correspond to the main output voltage of the DC/DC converter. (See the Self-Starting Architecture section.) After this preset interval has completed, the normal soft-start interval begins and the charging current is reduced to 5μA. The external soft-start voltage is used to internally ramp up the 0.6V reference (positive) input to the error amplifier. When fully charged, the RUN/SS voltage remains at 3V.

In the event that the sensed switch or inductor current exceeds the overcurrent trip threshold, an internal fault latch is tripped. When such a fault is detected, the LTC3726 immediately goes to zero duty cycle and initiates a soft-start retry. Prior to discharging the soft-start capacitor, however, the LTC3726 first puts a voltage pulse on the RUN/SS pin, which trips the fault latch in any other LTC3726 that shares the RUN/SS. This ensures an orderly shutdown of all phases in a PolyPhase application. After the soft-start capacitor is fully discharged, the LTC3726 attempts a restart. If the fault is persistent, the system enters a "hiccup" mode.

Note that in self-starting secondary-side control applications (with the LTC3705 or LTC3725), the presence of the LT3726 bias voltage is dependent upon the regular switching of the primary-side MOSFETs. Therefore, depending on the details of the application circuit, the LTC3726 may lose its bias voltage after a fault has been detected and before completing a soft-start retry. In this case, the "hiccup-mode" operation is actually governed by the LTC3705/LTC3725 soft-start circuitry (see the LTC3705/LTC3725 data sheets).

Drive Mode and Maximum Duty Cycle

Although the LTC3726 is primarily intended to be used with the LTC3705/LTC3725 in forward converter applications, the MODE pin provides the flexibility to use the LTC3726 in a wide variety of additional applications. This pin can be used to defeat the gate drive encoding scheme, as well as change the maximum duty cycle from its default value of 50%. The use of the MODE pin is summarized in Table 3.

When the gate drive encoding scheme is defeated, a standard PWM-style signal will be present at the PT^+ pin and a reference clock (in phase with the PWM signal) will be present at the PT^- pin. These outputs can be used in "standalone" applications (without the LTC3705/LTC3725) to drive the gates of MOSFETs in a conventional manner.

Table 3

MODE PIN	PT^+/PT^- Mode (MAX DUTY CYCLE)	INTENDED APPLICATION
GND	Encoded PWM (D_{MAX} = 50%)	2-Switch Forward with LTC3705
V_{CC}	Encoded PWM (D_{MAX} = 75%)	1-Switch Forward with LTC3725
200kΩ to GND	Standard PWM (D_{MAX} = 50%)	2-Switch Forward Standalone
100kΩ to GND	Standard PWM (D_{MAX} = 75%)	1-Switch Forward Standalone

Overvoltage Protection

This circuit monitors the voltage on the FB input. If the voltage on the FB pin exceeds 117% of 0.6V (0.7V), an overvoltage (OVP) is detected. For overvoltage protection, the secondary-side synchronous MOSFET is turned on while all other MOSFETs are turned off. This protection mode is not latched, so that the overvoltage detection is cleared if the FB voltage falls below 115% of 0.6V (0.69V).

OPERATION

Slave Mode Operation

When two or more LTC3726 devices are used in PolyPhase systems, one device becomes the "Master" controller, while the others are used as "Slaves." Slave mode is activated when the FB/PHASE pin is greater than approximately 2V. In this mode, the ITH pin becomes a high-impedance input, allowing it to be driven by the Master controller. In this way, equal inductor currents are established in each of the individual phases. Also, in slave mode, the soft-start charge/discharge currents are disabled, allowing the Master device to control the charging and discharging of the soft-start capacitor.

In slave mode, the phase angle of each LTC3726 can be set by using the FB/PHASE pin. This pin can be tied to V_{CC}, or have a single resistor to V_{CC} to activate Slave mode and set the phase angle (delay) of the internal oscillator relative to the incoming sync signal on the FS/SYNC pin. Any one of six preset values can be selected as summarized in Table 4.

Table 4

FB/PHASE PIN	PHASE DELAY	OPERATING MODE
$V_{FB/PHASE} < 2V$	0°	Master
$V_{FB/PHASE} = V_{CC}$	180°	Slave
200kΩ to V_{CC}	60°	Slave
100kΩ to V_{CC}	90°	Slave
50kΩ to V_{CC}	120°	Slave

APPLICATIONS INFORMATION

Start-Up Considerations

In self-starting applications, the LTC3705/LTC3725 will initially begin the soft-start of the converter in an open-loop fashion. After bias is obtained on the secondary side, the LTC3726 assumes control and completes the soft-start interval. In order to ensure that control is properly transferred from the LTC3705/LTC3725 (primary-side) to the LTC3726 (secondary-side), it is necessary to limit the rate of rise on the primary-side soft-start ramp so that the LTC3726 has adequate time to wake up and assume control before the output voltage gets too high. This condition is satisfied for many applications if the following relationship is maintained:

$$C_{SS,SEC} \leq C_{SS\ PRI}$$

However, care should be taken to ensure that soft-start transfer from primary-side to secondary-side is completed well before the output voltage reaches its target value. A good design goal is to have the transfer completed when the output voltage is less than one-half of its target value. Note that the fastest output voltage rise time during primary-side soft-start mode occurs with maximum input voltage and minimum load current.

The open-loop start-up frequency on the LTC3705/LTC3725 is set by placing a resistor from the FB/IN$^+$ pin to GND. Although the exact start-up frequency on the primary side is not critical, it is generally good practice to set this approximately equal to the operating frequency on the secondary side. The FS/IN$^-$ start-up resistor for the LTC3705/LTC3725 may be selected using the following:

$$f_{PRI}(Hz) = \frac{3.2 \bullet 10^{10}}{R_{FS/IN^-} + 10k}$$

In the event that the secondary-side circuitry fails to properly start up and assume control of switching, there are several fail-safe mechanisms to help avoid overvoltage conditions. First, the LTC3705/LTC3725 contains a volt-second clamp that will keep the primary-side duty cycle at a level that cannot produce an overvoltage condition. Second, the LTC3705/LTC3725 contains a time-out feature that will detect a FAULT if the LTC3726 fails to start up and deliver PWM signals to the primary side. Finally, the LTC3726 has an independent overvoltage detection circuit that will crowbar the output of the DC/DC converter using the synchronous MOSFET switch.

In the event that a short circuit is applied to the output of the DC/DC converter prior to start-up, the LTC3726 will generally not receive enough bias voltage to operate. In this case, the LTC3705/LTC3725 will detect a FAULT for

APPLICATIONS INFORMATION

one of two reasons: 1) the start-up time-out feature will be activated since the LTC3726 never sends signals to the primary side or 2) the primary-side overcurrent circuit will be tripped because of current buildup in the output inductor. In either case, the LTC3705/LTC3725 will initiate a shutdown followed by a soft-start retry. See the LTC3705/LTC3725 data sheets for further details.

Bias Supply Generation

Figure 2 shows a commonly used method of developing a V_{CC} bias supply for the LTC3726. During start-up, the circuit of Figure 2 uses a peak detector followed by a simple linear regulator to rapidly develop a V_{CC} voltage for the LTC3726. Note that this bias voltage must rise faster than the open-loop soft-start that is initiated by the LTC3705/LTC3725. This ensures that the LTC3726 begins switching and assumes control of the soft-start before the output voltage has risen substantially.

The value of R1 should be chosen to keep the peak charging current below the maximum (non-repetitive peak) rating of diode D1, but should otherwise be as small as

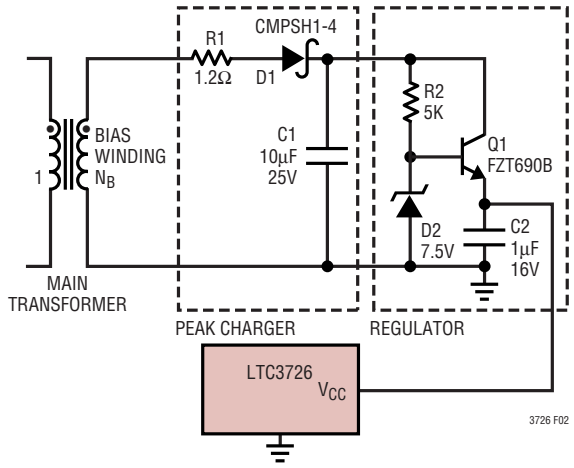


Figure 2. Typical Bias Supply Configuration

possible to provide a rapid charging of capacitor C1. This capacitor serves as a reservoir to provide bias voltage as the LTC3726 begins switching and assumes control of the soft-start from the LTC3705/LTC3725. Care should be taken to ensure that capacitor C1 is adequately large to provide enough hold-up time for the LTC3726 to assume control and establish a firm bias voltage at the main transformer.

The linear regulator of Figure 2 should be designed to handle the total expected I_{CC} current. For self-starting applications with the LTC3705/LTC3725, this regulator will supply the operating bias current for both primary and secondary side control circuitry. This current may be approximated using the following:

$$I_{CC} = I_{Q,3726} + M_S f_{OSC} Q_{G,SEC} + 2\left(M_P f_{OSC} Q_{G,PRI} + I_{Q,3705}\right) + I_{CORE} + 20 C_{SNUB} V_{CC} f_{OSC}$$

where $I_{Q,3705}$ and $I_{Q,3726}$ are the operating supply currents of the LTC3705/LTC3725 and LTC3706, M_P and M_S are the number of power MOSFETs used on the primary and secondary sides, $Q_{G,PRI}$ and $Q_{G,SEC}$ are the total gate charge of the primary and secondary MOSFETs, I_{CORE} is the core loss current associated with the pulse transformer, and C_{SNUB} is the snubber capacitor across the pulse transformer. Note that the current used by the primary side circuitry is doubled by the 2:1 turns ratio of the pulse transformer. For the Typical Application circuit of Figure 5, the total I_{CC} delivered by the linear regulator is 5mA + 3(50nC)(200kHz) + 2(2(38nC)(200kHz) + 2mA) + 3mA + 13mA = 85mA. To accommodate this current, Q1 should have a high Beta (>300), and R2 should be chosen to supply adequate base current at low V_{IN} (e.g., at 36V on the converter input), while maintaining a reasonable power dissipation in D2 at high V_{IN} (72V).

The turns ratio (N_B) of the bias winding should be chosen to ensure that there is adequate voltage to operate the LTC3726 over the entire range for the DC/DC converter's input bus voltage (V_{BUS}). This may be calculated using

$$N_B = \frac{V_{CC(MIN)} + 1.2V + \frac{R2 \cdot I_{CC}}{\beta_{Q1}}}{V_{BUS(MIN)}}$$

$V_{CC(MIN)}$ can be as low as 5V (if this provides adequate gate drive voltage to maintain acceptable efficiency), or as high as 7V. For the Figure 2 circuit if $V_{CC(MIN)}$ = 6V, I_{CC} = 85mA, and V_{BUS} = 36V-72V, this would mean a turns ratio N_B = 0.24, or a 9:2 transformer. Generally, if the output voltage of the DC/DC converter is 3.3V or higher, then the main output of the power transformer (tied to SW node on

APPLICATIONS INFORMATION

the LTC3726) can be used as the input to the peak charge circuit of Figure 2. For lower output voltages, however, it is normally necessary to use a dedicated bias winding to generate adequate bias voltage for the LTC3726.

Current Sensing

The LTC3726 provides considerable flexibility in current sensing techniques. It supports two main methods: 1) resistive current sensing and 2) current transformer current sensing. Resistive current sensing is generally simpler, smaller and less expensive, while current transformer sensing is more efficient and generally appropriate for higher (>20A) output currents. For resistive current sensing, the sense resistor may be placed in any one of three different locations: high side inductor, low side inductor or low side switch, as shown in Figure 3. Sensing the inductor current (high side or low side) is generally less noisy but dissipates more power than sensing the switch current (Figures 3a and 3b). High side inductor current sensing provides a more convenient layout than low side (no split ground plane), but can only be used for output voltages up to 5.5V, due to the common mode limitations of the current sense inputs (I_S^+ and I_S^-). For most applications, low side switch current sensing will be a good solution (Figure 3c).

For high current applications where efficiency (power dissipation) is very important, a current sense transformer may be used. As shown in Figure 3d, the I_S^- pin should be tied off to V_{CC} when a current sense transformer is used. This causes the I_S^+ pin to become a single ended (nondifferential) current sense input with a maximum current sense voltage of 1.28V. Figure 3d shows a typical application circuit using a current transformer.

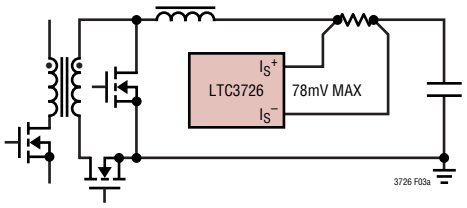


Figure 3a. High Side Inductor: Easier Layout, Low Noise, Accurate

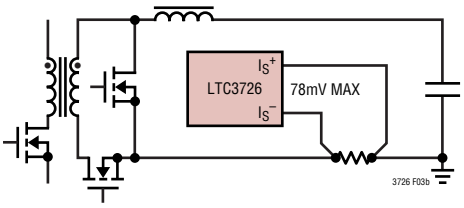


Figure 3b. Low Side Inductor: Accurate, Low Noise, High V_{OUT} Capable

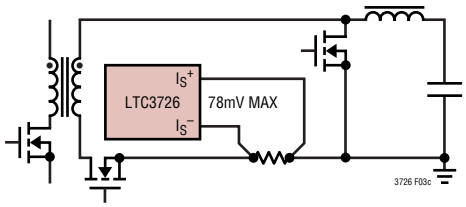


Figure 3c. Switch Current Sensing: Easy Layout, Accurate, Higher Efficiency, High V_{OUT} Capable

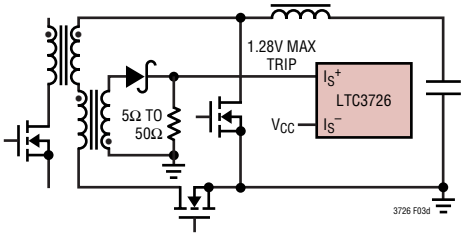


Figure 3d. Current Transformer: Highest Efficiency, High V_{OUT} Capable

Figure 3. Current Sensing Techniques

APPLICATIONS INFORMATION

PolyPhase Applications

Figure 4 shows the basic connections for using the LTC3705/LTC3725 and LTC3726 in PolyPhase applications. One of the phases is always identified as the "master," while all other phases are "slaves." For the LTC3705/LTC3725 (primary side), the master monitors the V_{IN} voltage for undervoltage, performs the open-loop start-up and supplies the initial V_{CC} voltage for the master and all slaves. The LTC3705/LTC3725 slaves simply stand by and wait for PWM signals from their respective pulse transformers. Since the SS/FLT pins of each master and slave LTC3705/LTC3725s are interconnected, a FAULT (overcurrent, etc.) on any one of the phases will perform a shutdown/restart on all phases together. The LTC3705/LTC3725 is put into slave mode by omitting the resistor on FS/IN^-. For the LTC3726, the master performs soft-start and voltage-loop regulation by driving all slaves to the same current as the master using the ITH pins. Faults and shutdowns are communicated via the interconnection of the RUN/SS pins. The LTC3726 is put into slave mode by tying the FB pin to V_{CC}.

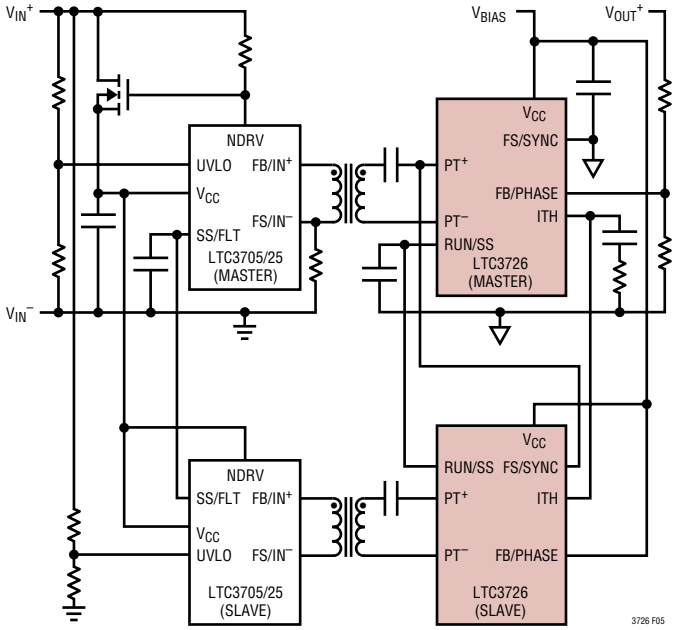
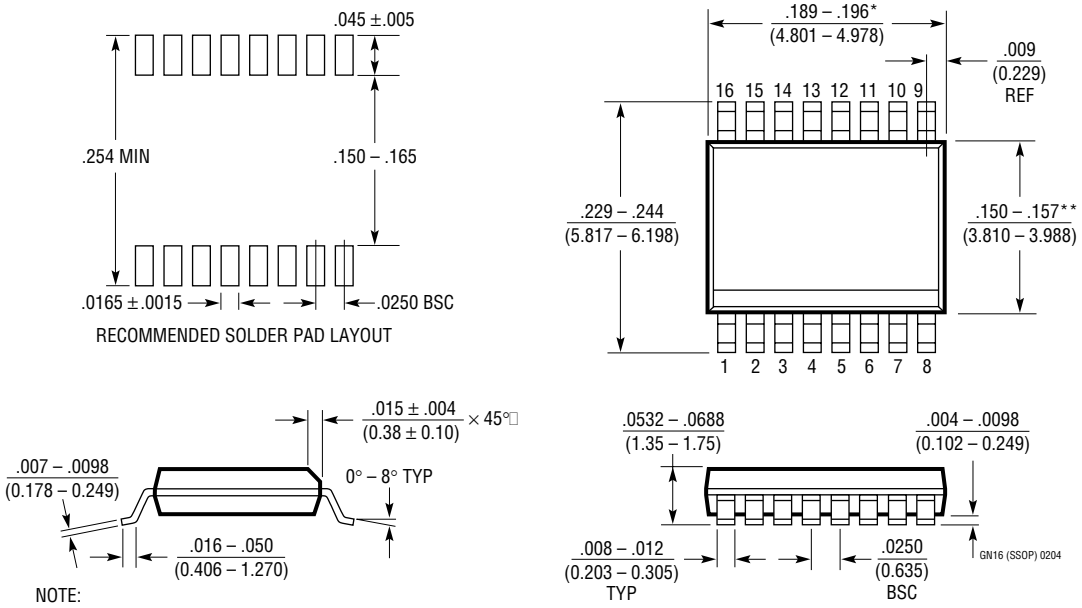


Figure 4. Connections for PolyPhase Operation

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

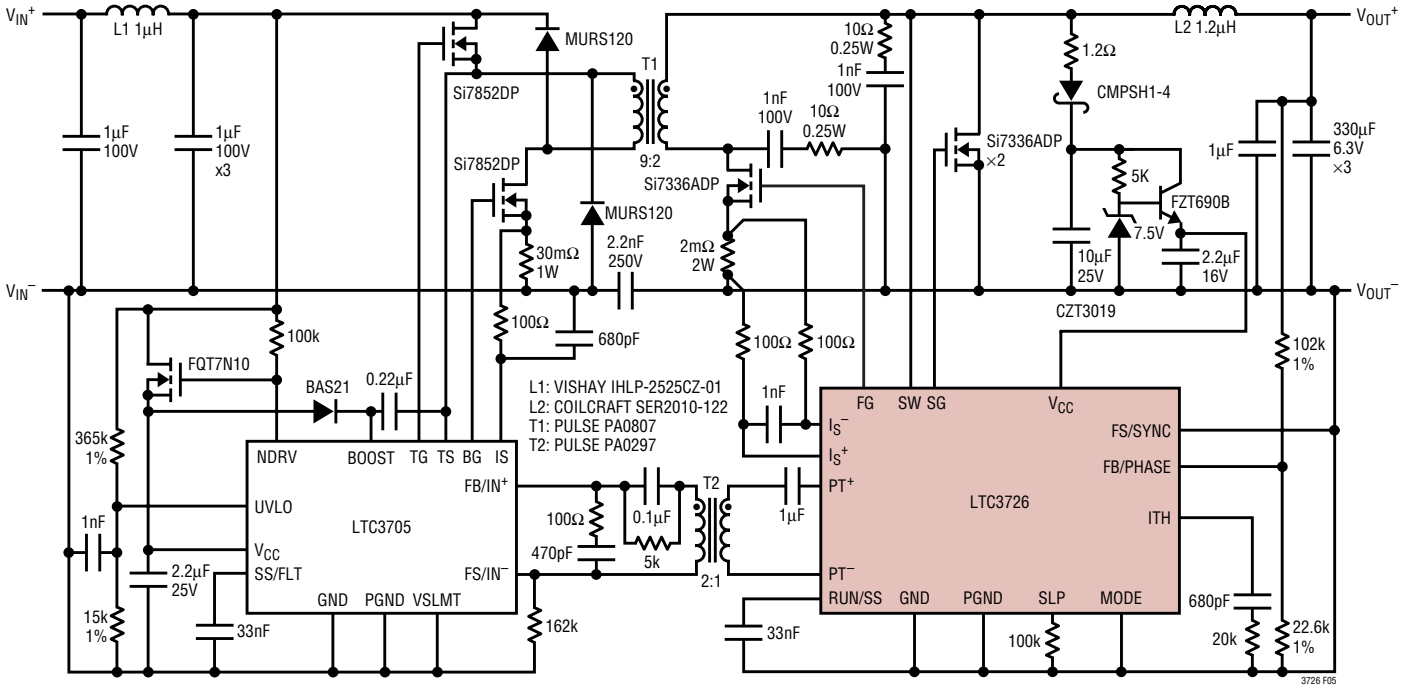


Figure 5. 36V-72V to 3.3V/20A Isolated Forward Converter (See Typical Performance Characteristics)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1534	Ultralow Noise 2A Switching Regulator	Reduces Conducted and Radiated EMI, Low Switching Harmonics, 20kHz to 250kHz Switching Frequency
LT1619	Low Voltage Current Mode Controller	$1.9V \le V_{IN} \le 18V$, 300kHz Operation, Boost, Flyback, SEPIC
LT1681/LT3781	Dual Transistor Synchronous Forward Controller	Operation Up to 72V Maximum
LT1725	General Purpose Isolated Flyback Controller	No Optoisolator Required, Accurate Regulation Without User Trims, 50kHz to 250kHz Switching Frequency, SSOP-16 Package
LTC1871	Wide Input Range, No R_{SENSE}™ Controller	Operation as Low as 2.5V Input, Boost, Flyback, SEPIC
LT1910	Protected High Side MOSFET Driver	8V to 48V Supply Range, Protected –15V to 60V Supply Transient
LT1952	Single Switch Forward Controller	25W to 500W; Synchronous Controller
LTC3440	Micropower Buck-Boost DC/DC Converter	Synchronous, Single Inductor, No Schottky Diode Required
LTC3704	Positive-to-Negative DC/DC Controller	$2.5V \le V_{IN} \le 36V$, No R_{SENSE} Current Mode Operation, Excellent Transient Response
LTC3705	Two-Switch Forward Converter Gate Driver and Controller	Use with LTC3726, Isolated Power Supplies, High Speed Gate Drivers
LT3706	PolyPhase Secondary Side Controller	Scalable Output Power; Self-Starting Architecture
LTC3722	Full Bridge Controller	Synchronous; ZVS Operation; 24-Pin SSOP
LTC3725	Two-Switch Forward Controller	On-Chip Gate-Driver; Fast Startup

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