PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES SEPTEMBER 7, 2016 **DATA SHEET**

## General Description

The ICS874003D-02 is a high performance Differential-to-LVDS Jitter Attenuator. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS874003D-02 has a bandwidth of 3MHz. The 3MHz provides an intermediate bandwidth that can easily track triangular spread profiles, while providing good jitter attenuation.

The ICS874003D-02 uses IDT's 3rd Generation FemtoClock® PLL technology to achieve the lowest possible phase noise. The device is packaged in a 20-Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-on cards.

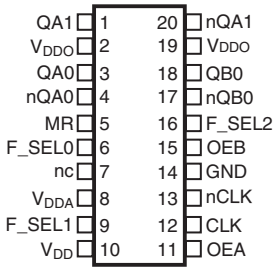
## Features

- Three differential LVDS output pairs
- One differential clock input
- CLK, nCLK can accept the following differential input levels: LVPECL, LVDS, HCSL
- Input frequency range: 98MHz to 128MHz
- Output frequency range: 98MHz to 320MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-Cycle jitter: 30ps (maximum)
- 3MHz PLL loop bandwidth
- 0°C to 70°C ambient operating temperature
- Full 3.3V operating supply
- Lead-free (RoHS 6) packaging
- For drop-in replacement use 874003AG-02

### F_SEL[2:0] Function Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| F_SEL2 | F_SEL1 | F_SEL0 | QA[0:1], nQA[0:1] | QB0, nQB0 |
| 0 | 0 | 0 | ÷2 (default) | ÷2 (default) |
| 1 | 0 | 0 | ÷5 | ÷2 |
| 0 | 1 | 0 | ÷4 | ÷2 |
| 1 | 1 | 0 | ÷2 | ÷4 |
| 0 | 0 | 1 | ÷2 | ÷5 |
| 1 | 0 | 1 | ÷5 | ÷4 |
| 0 | 1 | 1 | ÷4 | ÷5 |
| 1 | 1 | 1 | ÷4 | ÷4 |

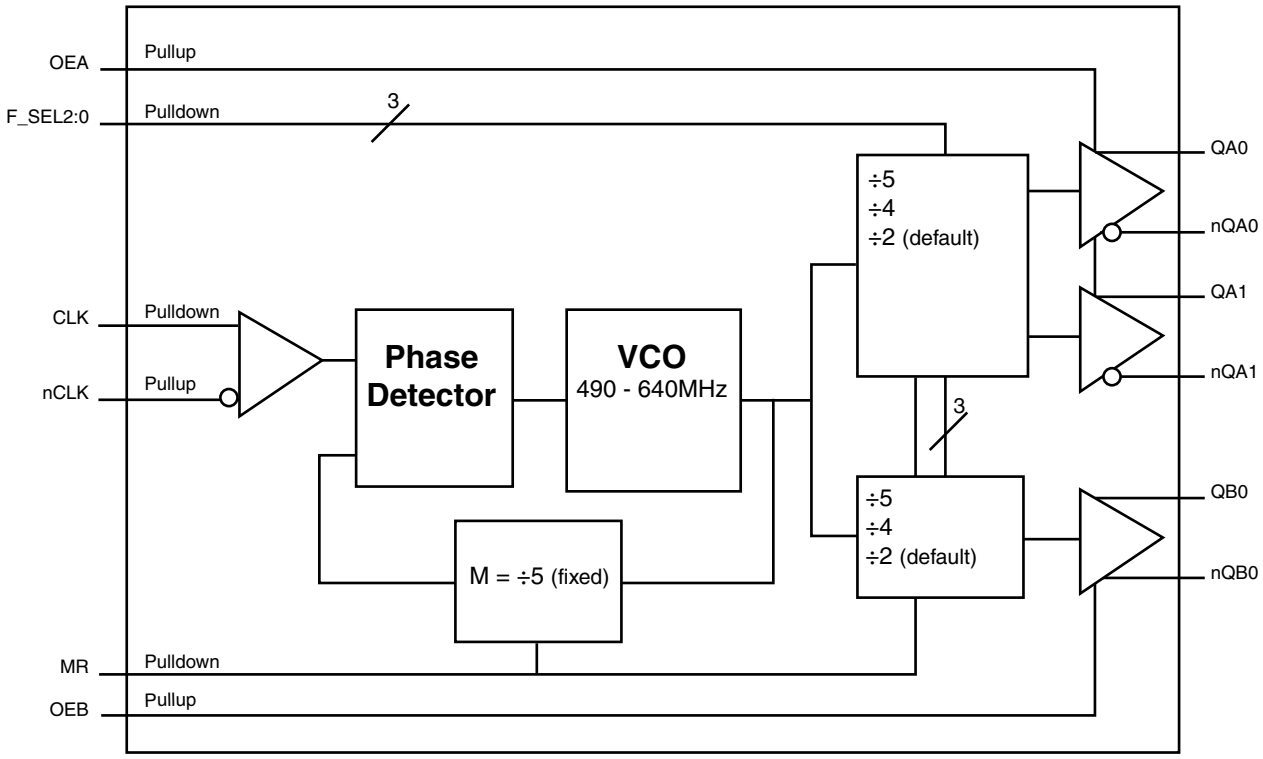
## Pin Assignment




**ICS874003D-02**
**20-Lead TSSOP**
**6.5mm x 4.4mm x 0.925mm package body**
**G Package**
**Top View**

## Block Diagram



# Pin Description and Pin Characteristic Tables

**Table 1. Pin Descriptions**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 20 | QA1, nQA1 | Output | | Differential output pair. LVDS interface levels. |
| 2, 19 | $V_{DDO}$ | Power | | Output supply pins. |
| 3, 4 | QA0, nQA0 | Output | | Differential output pair. LVDS interface levels. |
| 5 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 6, 9, 16 | F_SEL0, F_SEL1, F_SEL2 | Input | Pulldown | Frequency select pin for QAx, nQAx and QB0, nQB0 outputs. LVCMOS/LVTTL interface levels. |
| 7 | nc | Unused | | No connect. |
| 8 | $V_{DDA}$ | Power | | Analog supply pin. |
| 10 | $V_{DD}$ | Power | | Core supply pin. |
| 11 | OEA | Input | Pullup | Output enable pin for QAx pins. When HIGH, the QAx, nQAx outputs are active. When LOW, the QAx, nQAx outputs are in a high impedance state. LVCMOS/LVTTL interface levels. |
| 12 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 13 | nCLK | Input | Pullup | Inverting differential clock input. |
| 14 | GND | Power | | Power supply ground. |
| 15 | OEB | Input | Pullup | Output enable pin for QB0 pins. When HIGH, the QB0, nQB0 outputs are active. When LOW, the QB0, nQB0 outputs are in a high impedance state. LVCMOS/LVTTL interface levels. |
| 17, 18 | nQB0, QB0 | Output | | Differential output pair. LVDS interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

**Table 2. Pin Characteristics**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

# Function Table

**Table 3. Output Enable Function Table**

| Inputs | | Outputs | |
|---|---|---|---|
| **OEA** | **OEB** | **QA[0:1], nQA[0:1]** | **QB0, nQB0** |
| 0 | 0 | Hi-Impedance | Hi-Impedance |
| 1 | 1 | Enabled | Enabled |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current | <br>10mA<br>15mA |
| Package Thermal Impedance, $\theta_{JA}$ | 86.7°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. LVDS Power Supply DC Characteristics,** $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A$ = 0°C to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD}$ – 0.15 | 3.3 | $V_{DD}$ | V |
| $V_{DDO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | | 80 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 15 | mA |
| $I_{DDO}$ | Output Supply Current | | | | 75 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A$ = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | OEA, OEB | $V_{DD} = V_{IN} = 3.465V$ | | | 5 | µA |
| | | MR, F_SEL[2:0] | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | OEA, OEB | $V_{DD} = 3.465V$, $V_{IN} = 0V$ | -150 | | | µA |
| | | MR, F_SEL[2:0] | $V_{DD} = 3.465V$, $V_{IN} = 0V$ | -5 | | | µA |

**Table 4C. Differential DC Characteristics,** $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | nCLK | $V_{DD} = V_{IN} = 3.465V$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK | $V_{DD} = 3.465V$, $V_{IN} = 0V$ | -5 | | | µA |
| | | nCLK | $V_{DD} = 3.465V$, $V_{IN} = 0V$ | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | GND + 0.5 | | $V_{DD} – 0.85$ | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as $V_{IH}$.

**Table 4D. LVDS DC Characteristics,** $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 275 | 375 | 485 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | 1.2 | 1.35 | 1.5 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

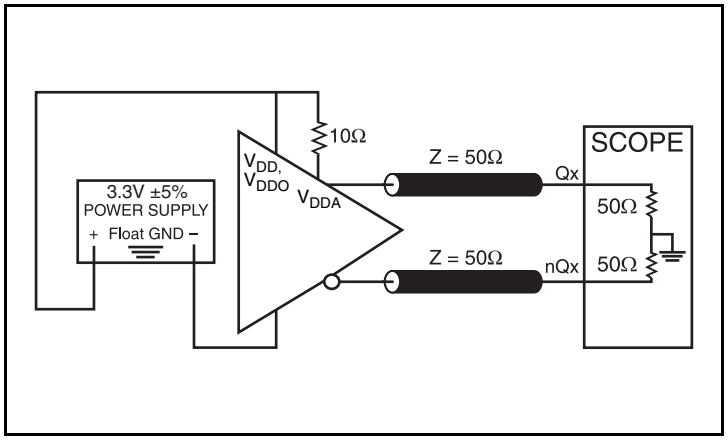
**Table 5. AC Characteristics,** $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | 98 | | 320 | MHz |
| *t*jit(cc) | Cycle-to-Cycle Jitter; NOTE 1 | | | | 30 | ps |
| *tsk*(o) | Output Skew; NOTE 2, 3 | | | | 185 | ps |
| *tsk*(b) | Bank Skew; NOTE 1, 4 | Bank A | | | 65 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 250 | | 700 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

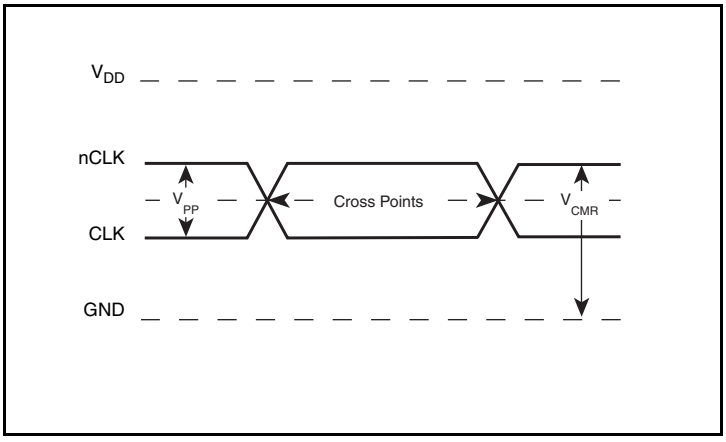
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

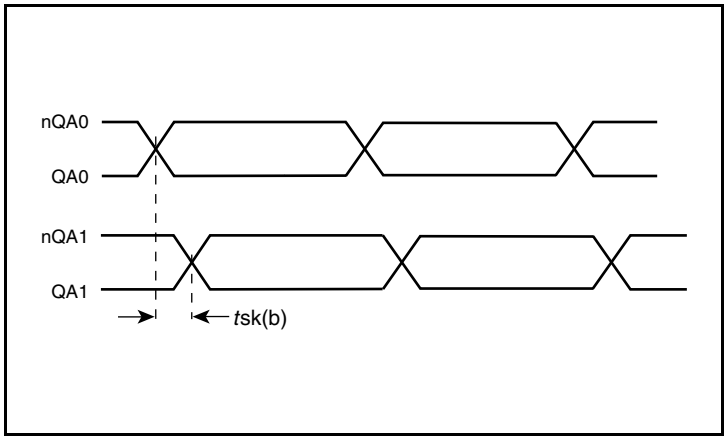
# Parameter Measurement Information



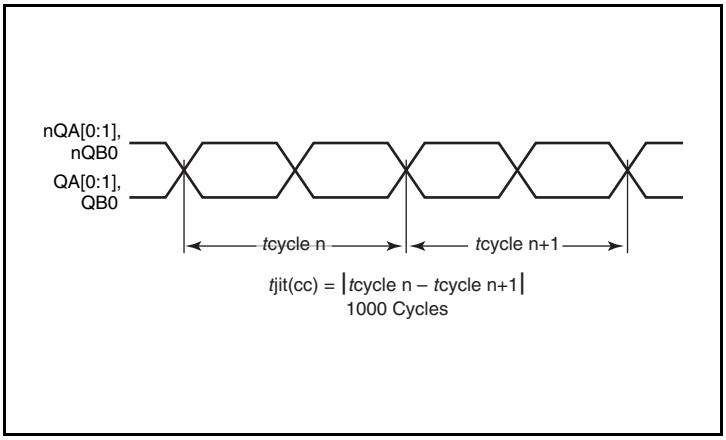

**3.3V LVDS Output Load Test Circuit**



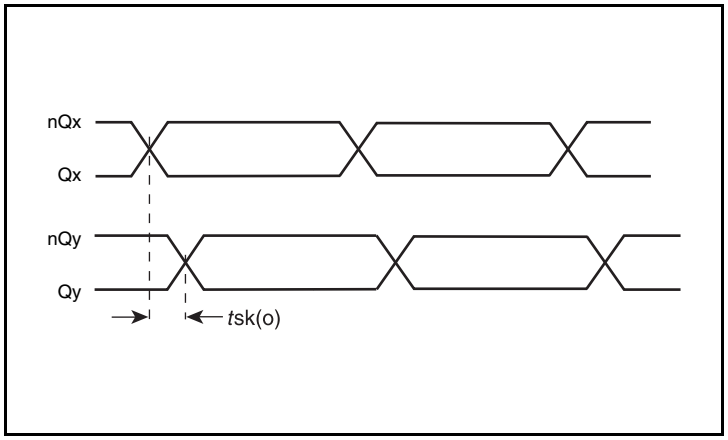

**Differential Input Level**



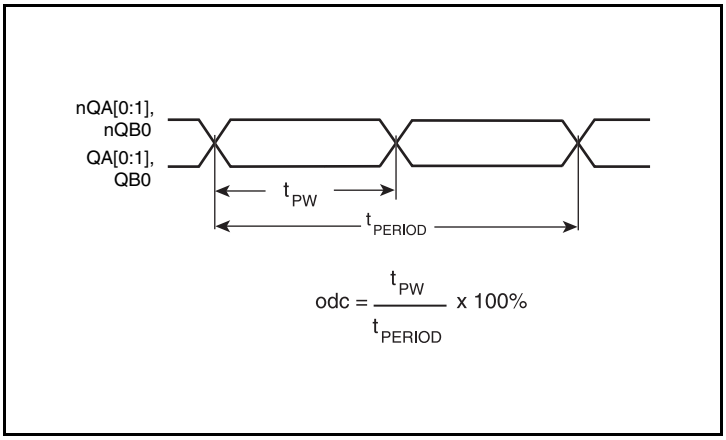

**Bank Skew**




**Cycle-to-Cycle Jitter**



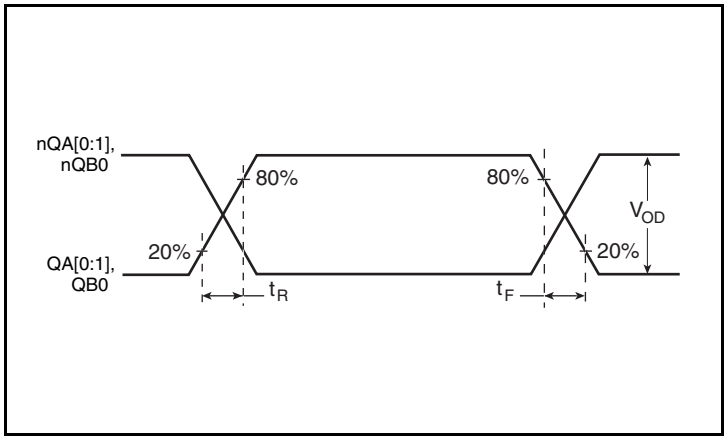

**Output Skew**



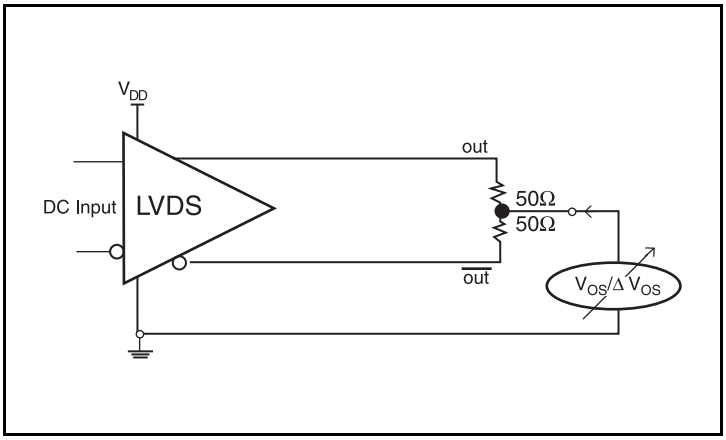

**Output Duty Cycle/Pulse Width/Period**

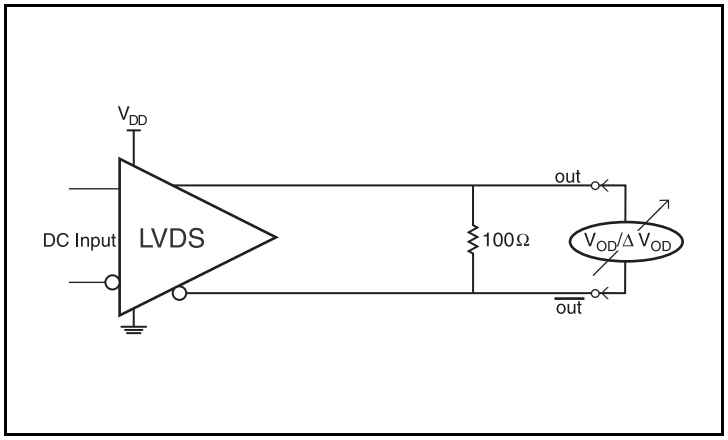
## Parameter Measurement Information, continued




**Output Rise/Fall Time**




**Offset Voltage Setup**




**Differential Output Voltage Setup**

# Applications Information

## Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_1$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC}$ = 3.3V, R1 and R2 value should be adjusted to set $V_1$ at 1.25V. The values below are for when both the single ended swing and $V_{CC}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{CC}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

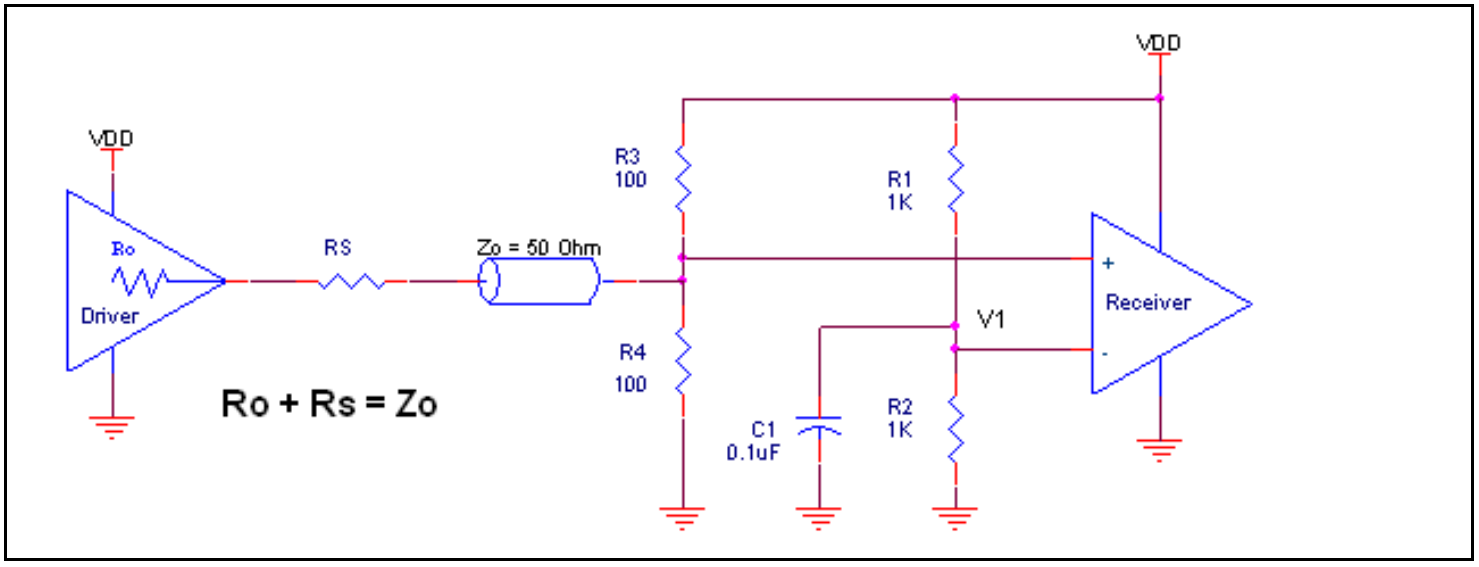



**Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. The differential signal must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 2A* to *2D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

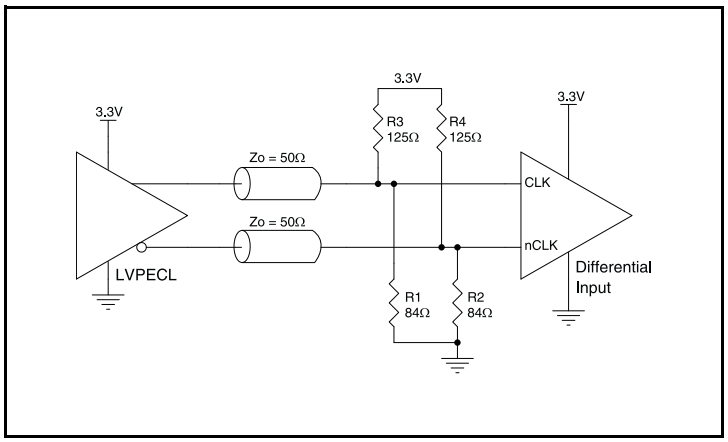



**Figure 2A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

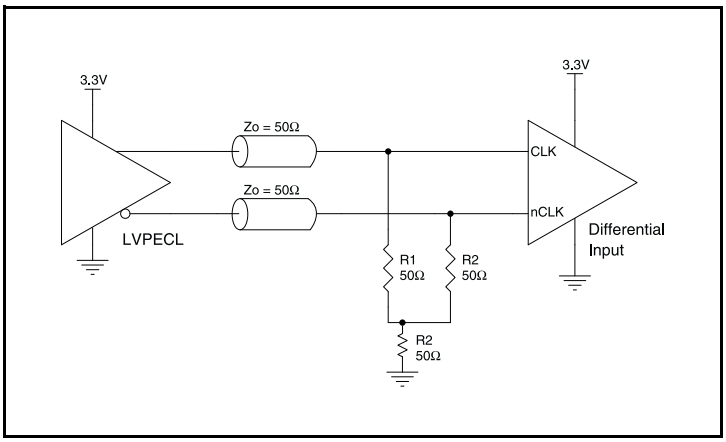



**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

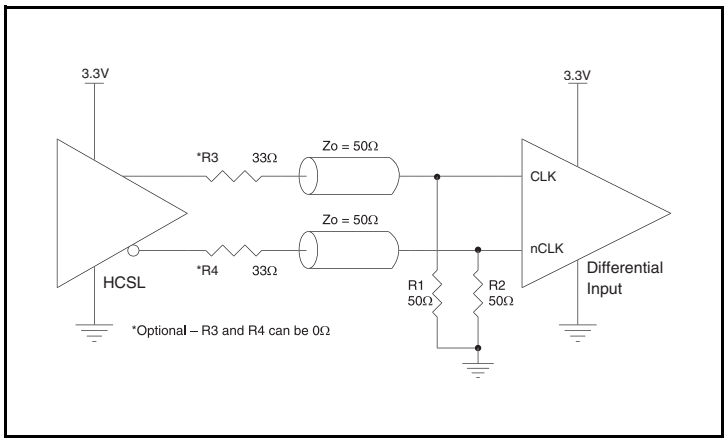



**Figure 2C. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

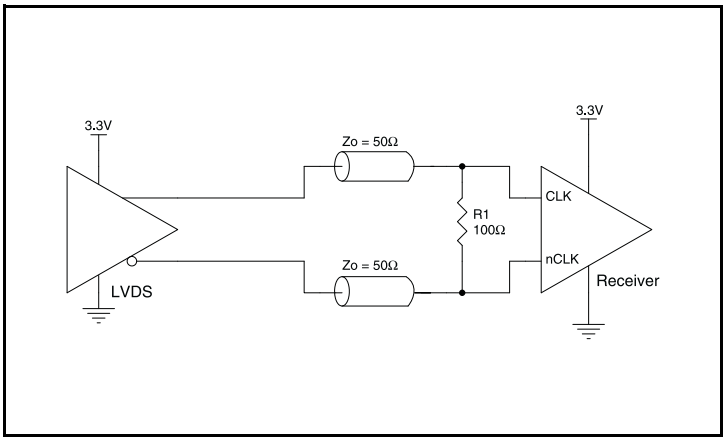



**Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ($Z_T$) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ($Z_0$) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

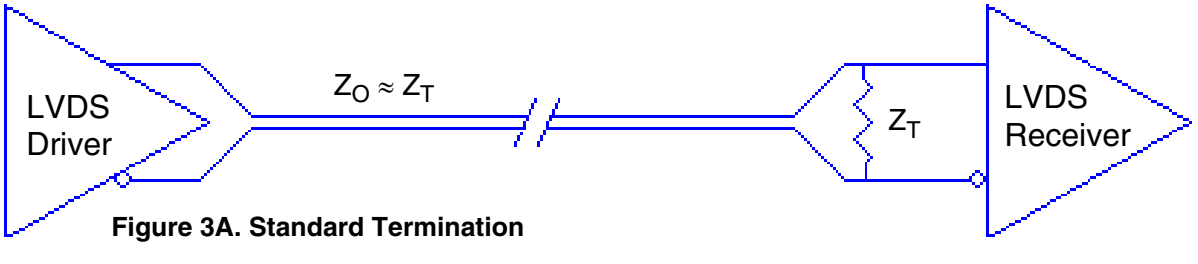



**Figure 3A. Standard Termination**

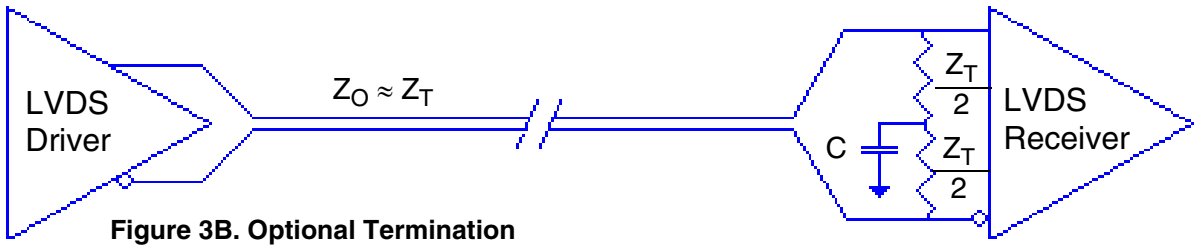



**Figure 3B. Optional Termination**

**LVDS Termination**

## Schematic Layout

*Figure 4* shows an example of ICS874003D-02 application schematic. This example focuses on functional connections and is not configuration specific. In this example, the device is operated at $V_{DD} = V_{DDO} = 3.3V$. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For the LVDS output drivers, two termination examples are shown in the schematic.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS874003D-02 provides separate $V_{DD}$, $V_{DDA}$ and $V_{DDO}$ power supplies to isolate any high switching noise from coupling into the internal oscillator. In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors on the device side of the ferrite beads be placed on the device side of the PCB as close to the power pins as possible.This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10µF and 0.1µF capacitor connected to the board supplies can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

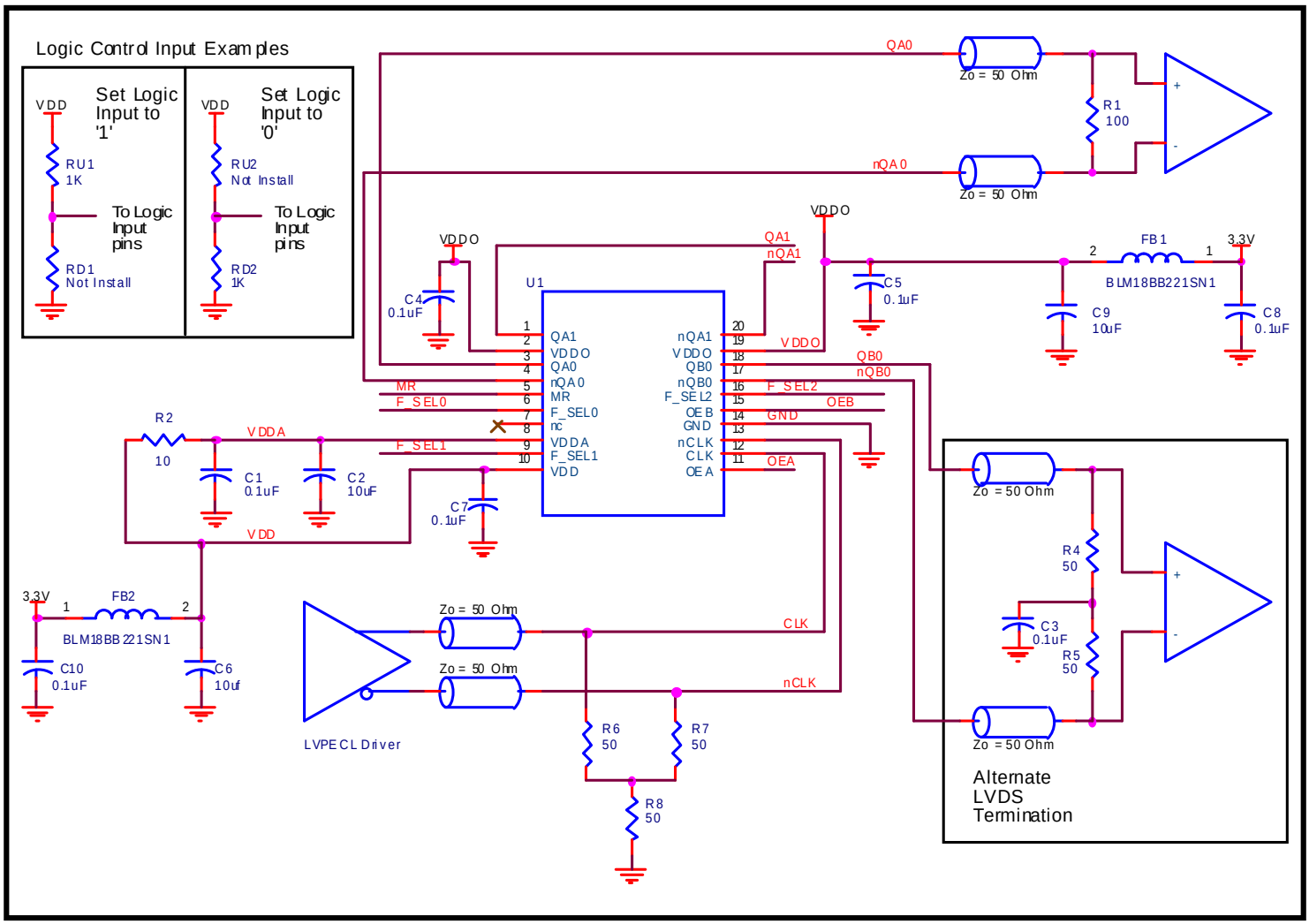



**Figure 4. ICS874003D-02 Schematic Layout**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS874003D-02.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS74003D-02 is the sum of the core power plus the analog power plus the power dissipated due to the load. The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (80mA + 15mA) = **329.175mW**
- Power $(outputs)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX}$ = 3.465V * 75mA = **259.87mW**

**Total Power**$_{\_MAX}$ = 329.175mW + 259.87mW = **589.045mW**

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### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 86.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.589W * 86.7°C/W = 121.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance $\theta_{JA}$ for 20-Lead TSSOP, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 86.7°C/W | 82.4°C/W | 80.2°C/W |

 

# Reliability Information

**Table 7. $\theta_{JA}$ vs. Air Flow Table for a 20-Lead TSSOP**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 86.7°C/W | 82.4°C/W | 80.2°C/W |

## Transistor Count

The transistor count for ICS874003D-02 is: 1408

# Package Outline and Package Dimensions

**Package Outline - G Suffix for 20-Lead TSSOP**

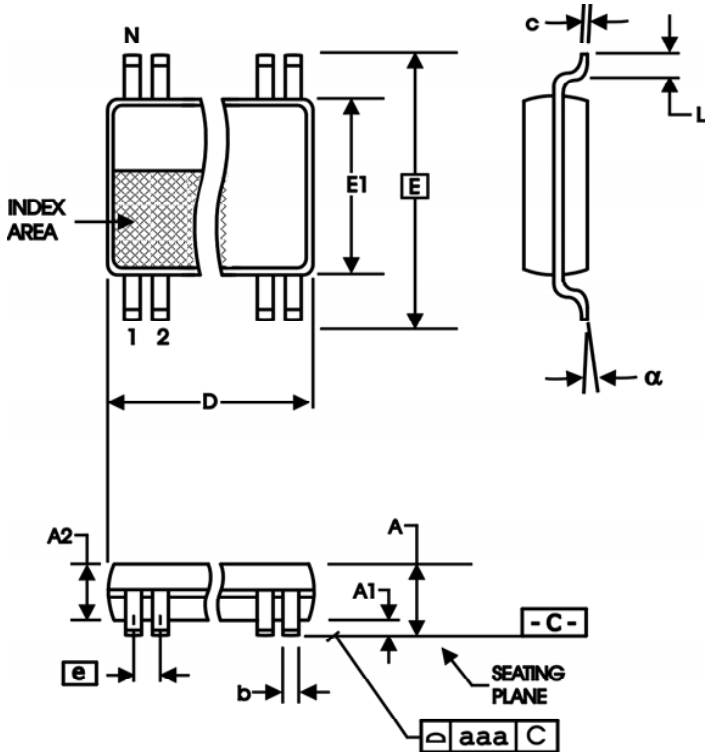


**Table 8. Package Dimensions**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 20 | |
| **A** | | 1.20 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.80 | 1.05 |
| **b** | 0.19 | 0.30 |
| **c** | 0.09 | 0.20 |
| **D** | 6.40 | 6.60 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.45 | 0.75 |
| $\alpha$ | 0° | 8° |
| **aaa** | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

 

# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 874003DG-02LF | ICS74003D02L | “Lead-Free” 20-Lead TSSOP | Tube | 0°C to 70°C |
| 874003DG-02LFT | ICS74003D02L | “Lead-Free” 20-Lead TSSOP | Tape & Reel | 0°C to 70°C |

# Revision History

3/11/16 Product Discontinuation Notice - Last time buy expires September 7, 2016.
PDN N-16-02

 

# We've Got Your Timing Solution

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

**Sales**
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

**Technical Support Sales**
clocks@idt.com
+480-763-2056