VMMK-2503

1 to 12 GHz GaAs Wideband Amplifier in Wafer Level Package

Data Sheet

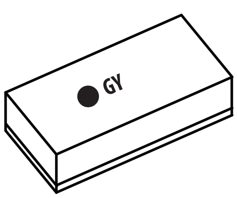
Lead (Pb) Free
RoHS 6 fully
compliant

Description

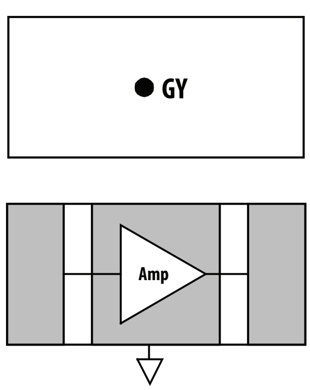
Avago's VMMK-2503 is an easy-to-use broadband, high linearity amplifier in a miniaturized wafer level package (WLP). The wide band and unconditionally stable performance makes this amplifier suitable as a gain block or a transmitter driver in many applications from 1–12GHz. A 5V, 65mA power supply is required for optimal performance.

This amplifier is fabricated with enhancement E-pHEMT technology and industry leading wafer level package. The GaAsCap wafer level package is small and ultra thin yet can be handled and placed with standard 0402 pick and place assembly. This product is easy to use since it requires only positive DC voltages for bias and no matching coefficients are required for impedance matching to 50 Ω systems.

WLP 0402, 1mm x 0.5mm x 0.25 mm



Pin Connections (Top View)



Note:
"G" = Device Code
"Y" = Month Code

Features

- 1 x 0.5 mm Surface Mount Package
- Ultrathin (0.25mm)
- Unconditionally Stable
- Ultrawide Bandwidth
- Gain Block or Driver Amplifier
- RoHS6 + Halogen Free

Typical Performance (Vdd = 5.0V, Idd = 65mA)

- Output IP3: 27dBm
- Small-Signal Gain: 13.5dB
- Noise Figure: 3.4dB

Applications

- 2.4 GHz, 3.5GHz, 5-6GHz WLAN and WiMax notebook computer, access point and mobile wireless applications
- 802.16 & 802.20 BWA systems
- Radar, radio and ECM systems
- UWB

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 60V
ESD Human Body Model = 625V
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

Table 1. Absolute Maximum Ratings [1]

Sym	Parameters/Condition	Unit	Absolute Max
Vd	Supply Voltage (RF Output) [2]	V	6
Id	Device Current [2]	mA	120
$P_{in, max}$	CW RF Input Power (RF Input) [3]	dBm	+20
P_{diss}	Total Power Dissipation	mW	720
Tch	Max channel temperature	°C	150
θjc	Thermal Resistance [4]	°C/W	140

Notes
1. Operation in excess of any of these conditions may result in permanent damage to this device.
2. Bias is assumed DC quiescent conditions
3. With the DC (typical bias) and RF applied to the device at board temperature Tb = 25°C
4. Thermal resistance is measured from junction to board using IR method

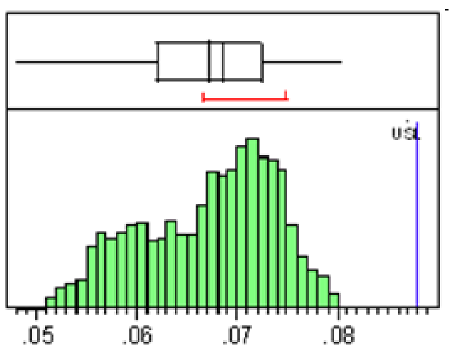
Table 2. DC and RF Specifications

T_A= 25°C, Frequency = 6 GHz, Vd = 5V, $Z_{in} = Z_{out}$ = 50Ω (unless otherwise specified)

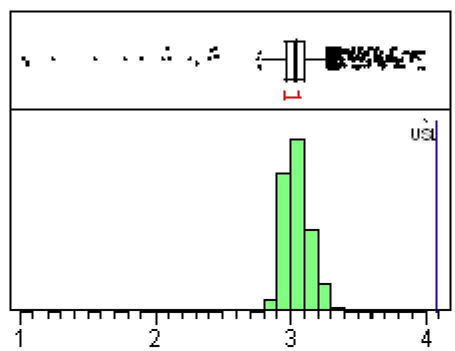
Sym	Parameters/Condition	Unit	Minimum	Typ.	Maximum
Id	Device Current	mA	46	68	88
NF[1,2]	Noise Figure	dB	–	3.04	4.1
Ga [1,2]	Associated Gain	dB	12.5	13.5	18
OIP3 [1,2,3]	Output 3rd Order Intercept	dBm		+27	–
P-1dB[1,2]	Output Power at 1dB Gain Compression	dBm		+17	–
IRL [1,2]	Input Return Loss	dB	–	-14	–
ORL [1,2]	Output Return Loss	dB	–	-20	–

Notes:
1. Losses of test systems have been de-embedded from final data
2. Measure Data obtained from wafer-probing
3. OIP3 test condition: F1 = 6.0GHz, F2 = 6.01GHz, Pin = -20dBm

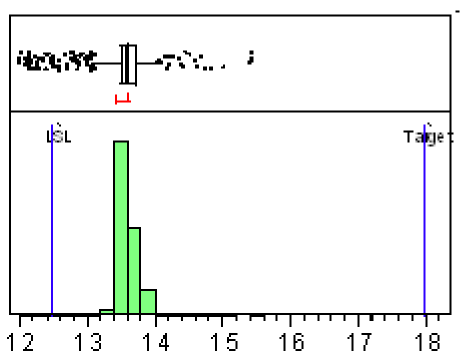
Product Consistency Distribution Charts at 6.0 GHz, Vd = 5 V



Id @ 5V, Mean=68mA, USL=88mA



NF@ 6GHZ, Mean=3.04dB, USL=4.1dB



Gain @ 6GHz, Mean=13.5dB, LSL=12.5dB, USL=18dB

Note: Distribution data based on ~50Kpcs sample size from MPV lots.

VMMK-2503 Typical Performance

(T_A = 25°C, Vdd = 5V, Idd = 65mA, Z_{in} = Z_{out} = 50 Ω unless noted)

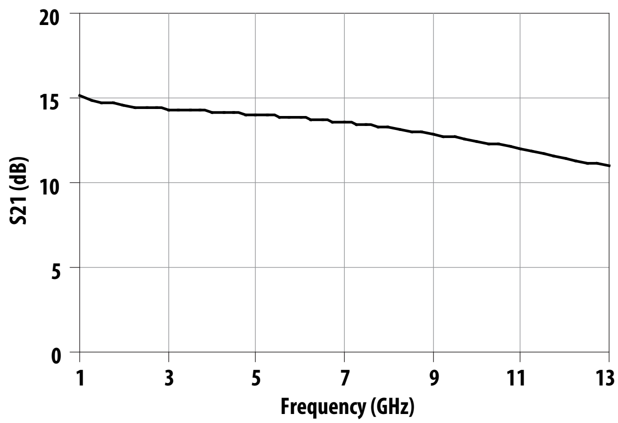


Figure 1. Small-signal Gain [1]

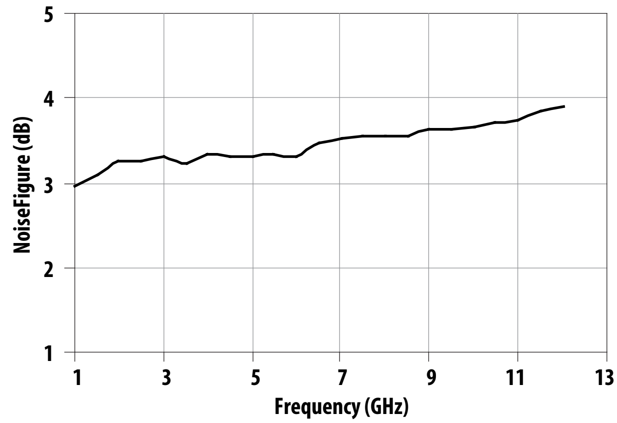


Figure 2. Noise Figure [1]

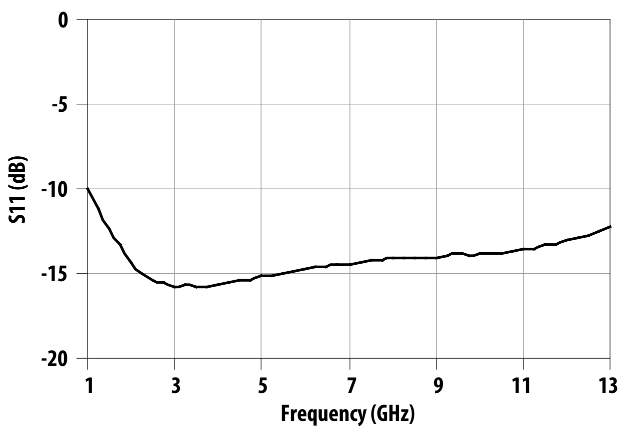


Figure 3. Input Return Loss [1]

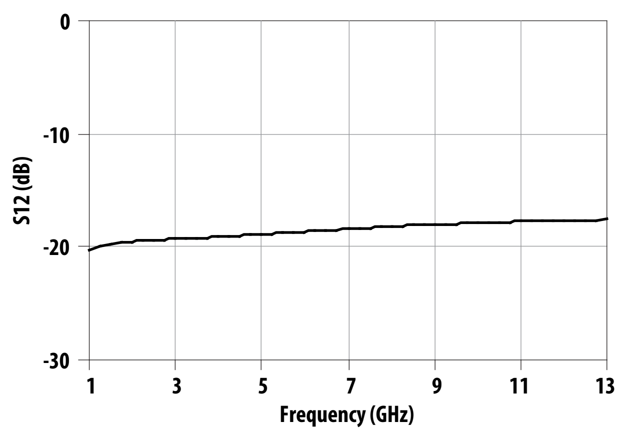


Figure 4. Isolation [1]

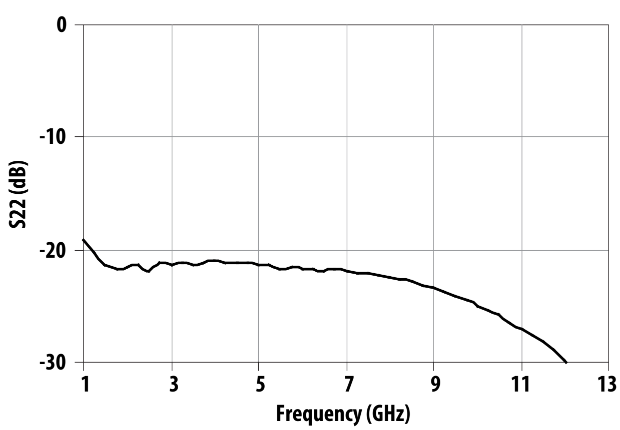


Figure 5. Output Return Loss [1]

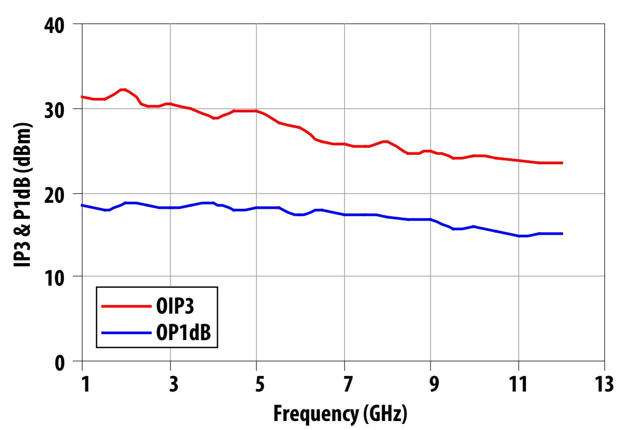


Figure 6. Output IP3 [1,2]

Notes:

1. Data taken on a G-S-G probe substrate fully de-embedded to the reference plane of the package
2. Output IP3 data taken at Pin=-15dBm

VMMK-2503 Typical Performance (continue)

(T_A = 25°C, Vdd = 5V, Idd = 65mA, Z_{in} = Z_{out} = 50 Ω unless noted)

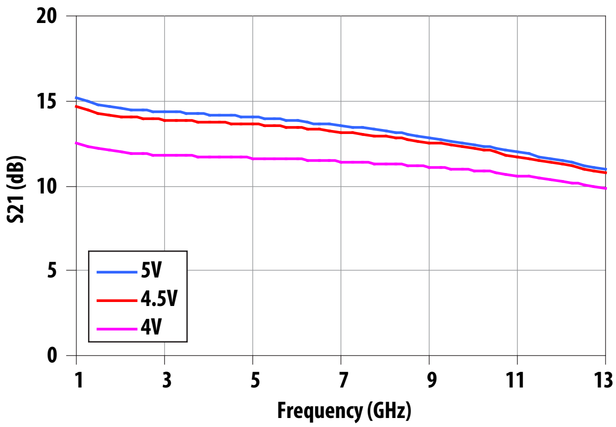


Figure 7. Gain over Vdd [1]

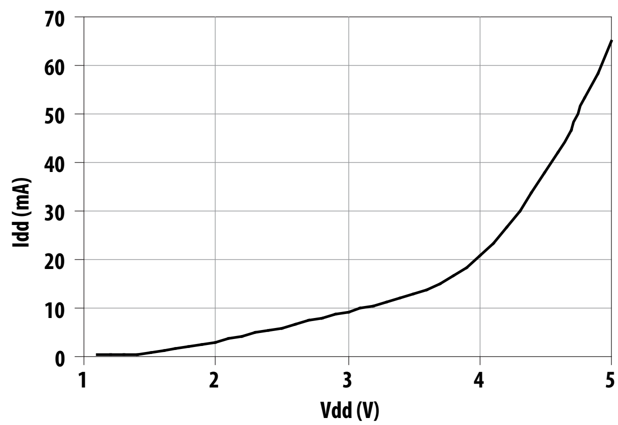


Figure 8. Total Current [1]

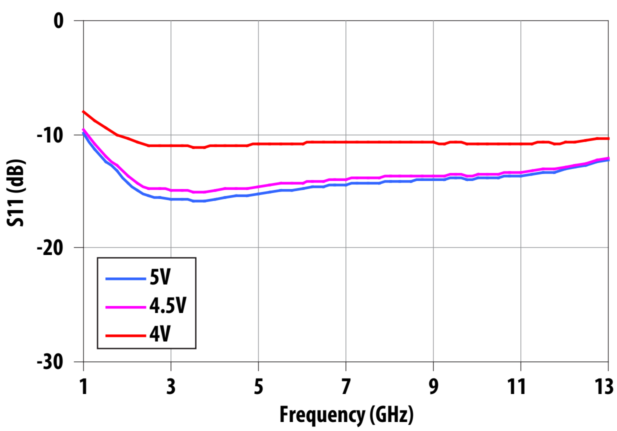


Figure 9. Input Return Loss over Vdd [1]

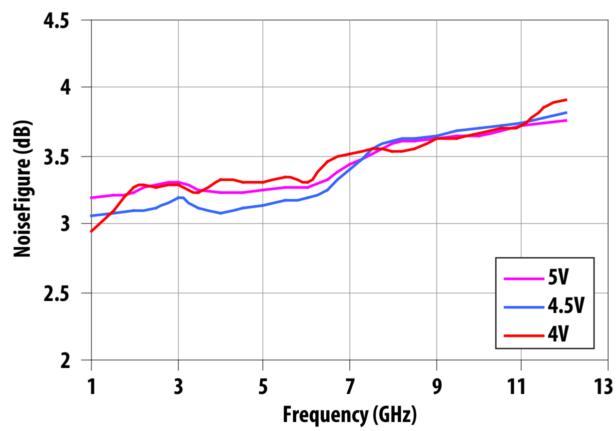


Figure 10. Noise Figure over Vdd [1]

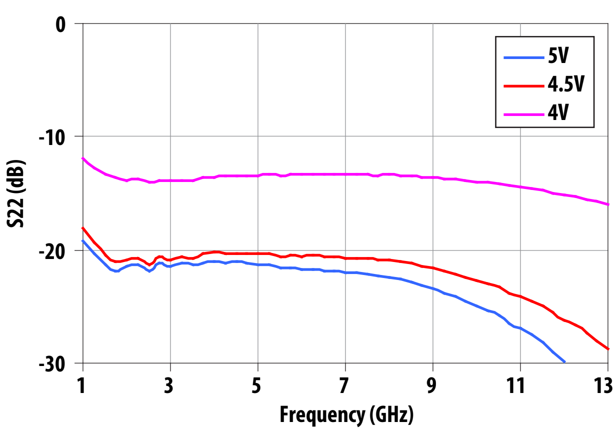


Figure 11. Output Return Loss Over Vdd [1]

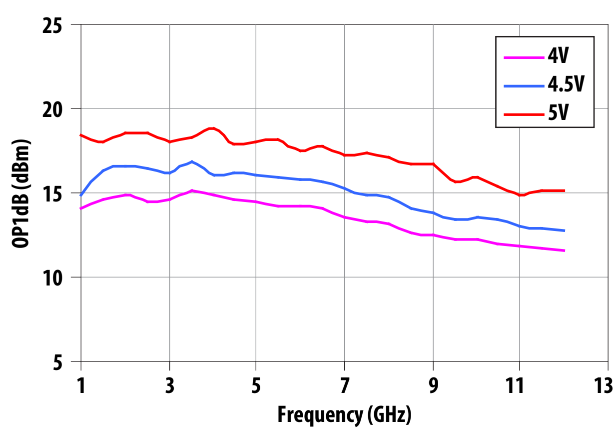


Figure 12. Output P1dB Over Vdd [1]

Note:

1. Data taken on a G-S-G probe substrate fully de-embedded to the reference plane of the package

VMMK-2503 Typical Performance (continue)

(T_A = 25°C, Vdd = 5V, Idd = 65mA, $Z_{in} = Z_{out}$ = 50 Ω unless noted)

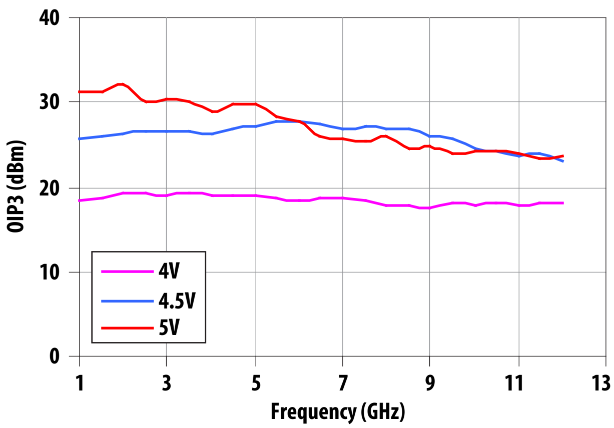


Figure 13. Output P1dB over Temp [3]

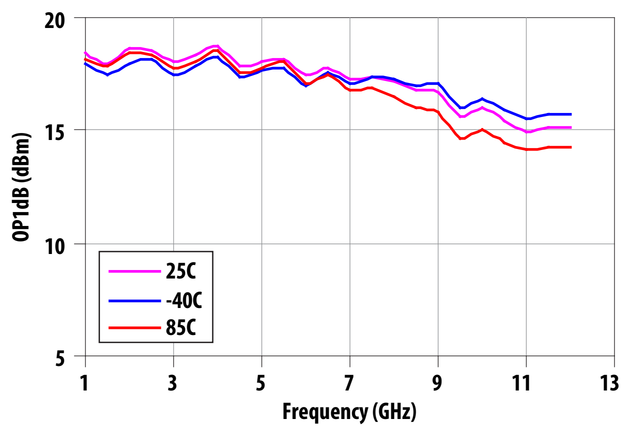


Figure 14. Output IP3 over Vdd [1,2]

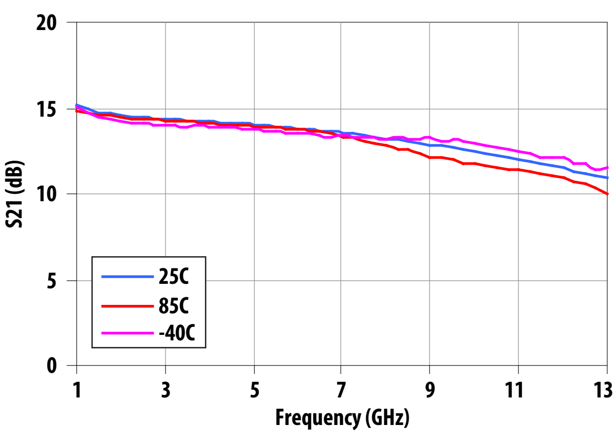


Figure 15. Gain over Temp [3]

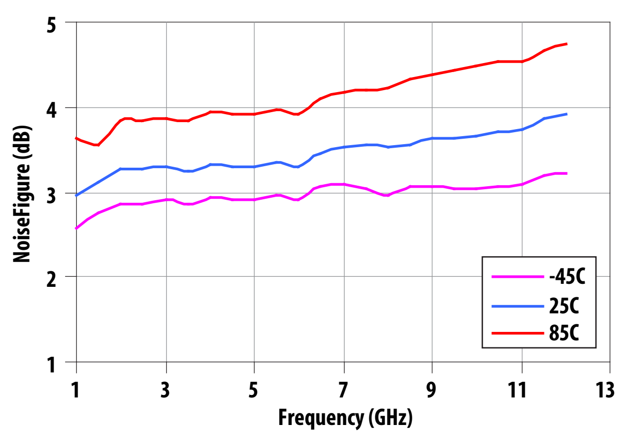


Figure 16. Noise Figure over Temp [3]

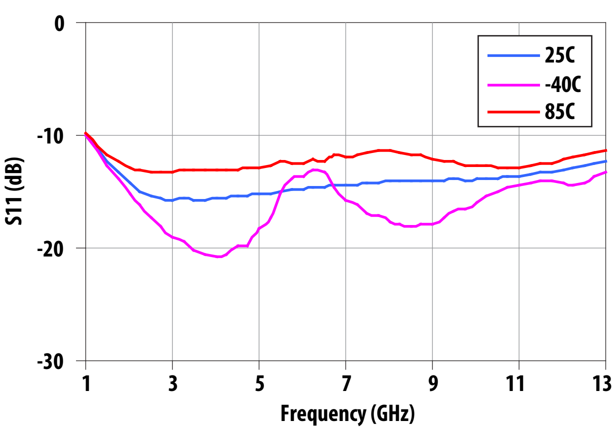


Figure 17. Input Return Loss Over Temp [3]

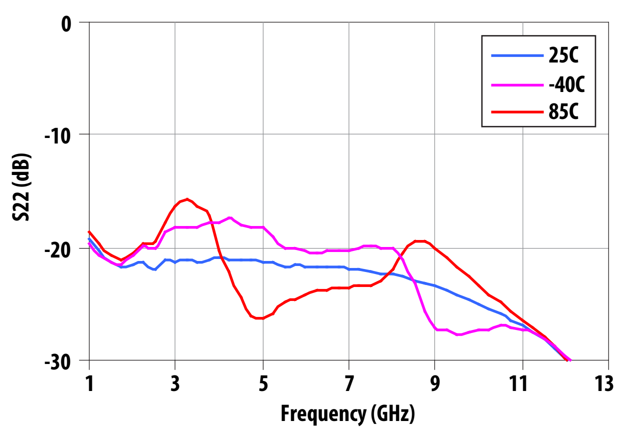


Figure 18. Output Return Loss Over Temp [3]

Notes:

1. Data taken on a G-S-G probe substrate fully de-embedded to the reference plane of the package
2. Output IP3 data taken at Pin=-15dBm
3. Over temp data taken on a test fixture (Figure 20) without de-embedding

VMMK-2503 Typical S-parameters

(T_A = 25°C, Vdd = 5V, Idd = 65mA, Z_{in} = Z_{out} = 50 Ω unless noted)

Freq GHz	S11			S21			S12			S22		
	Mag	dB	Phase	Mag	dB	Phase	Mag	dB	Phase	Mag	dB	Phase
1	0.32	-9.94	-58.82	5.73	15.16	157.97	0.10	-20.26	17.70	0.11	-19.18	-82.09
2	0.19	-14.31	-63.36	5.34	14.54	146.59	0.10	-19.58	6.88	0.08	-21.51	-116.84
3	0.16	-15.75	-62.41	5.22	14.35	133.94	0.11	-19.32	1.32	0.09	-21.40	-127.88
4	0.17	-15.65	-68.23	5.13	14.20	120.62	0.11	-19.14	-2.44	0.09	-20.96	-135.63
5	0.17	-15.19	-75.79	5.02	14.02	106.87	0.11	-18.91	-5.92	0.09	-21.32	-144.09
6	0.18	-14.78	-87.11	4.90	13.80	93.04	0.12	-18.67	-9.42	0.08	-21.68	-155.26
7	0.19	-14.44	-99.64	4.75	13.54	79.16	0.12	-18.45	-13.07	0.08	-21.97	-166.36
8	0.20	-14.12	-114.81	4.58	13.23	65.36	0.12	-18.22	-17.02	0.08	-22.44	-177.07
9	0.20	-14.04	-131.20	4.40	12.87	51.67	0.13	-18.04	-21.15	0.07	-23.45	171.57
10	0.20	-13.87	-150.35	4.19	12.44	38.17	0.13	-17.87	-25.41	0.06	-25.01	159.23
11	0.21	-13.60	-169.56	3.97	11.98	24.99	0.13	-17.74	-29.85	0.04	-26.97	144.70
12	0.22	-13.03	169.40	3.75	11.48	12.06	0.13	-17.67	-34.27	0.03	-29.82	128.66
13	0.24	-12.24	149.90	3.53	10.94	-0.50	0.13	-17.60	-38.63	0.02	-33.72	105.68
14	0.27	-11.38	131.14	3.30	10.38	-12.65	0.13	-17.58	-43.09	0.01	-38.20	58.43
15	0.30	-10.41	115.07	3.09	9.79	-24.56	0.13	-17.53	-47.40	0.01	-37.52	-7.15
16	0.34	-9.46	99.90	2.88	9.19	-36.14	0.13	-17.52	-51.43	0.02	-35.60	-43.96
17	0.37	-8.69	86.76	2.68	8.57	-47.41	0.13	-17.48	-55.43	0.02	-34.56	-75.88
18	0.40	-7.97	74.14	2.50	7.95	-58.26	0.14	-17.38	-59.63	0.02	-32.77	-114.10
19	0.43	-7.25	63.67	2.33	7.33	-68.81	0.14	-17.30	-63.51	0.04	-29.02	-141.61
20	0.46	-6.81	53.97	2.17	6.73	-79.06	0.14	-17.17	-67.56	0.05	-25.71	-158.63
21	0.48	-6.34	44.61	2.03	6.14	-89.16	0.14	-16.98	-71.95	0.07	-23.24	-171.34
22	0.50	-5.99	36.42	1.90	5.56	-99.02	0.14	-16.80	-76.07	0.09	-21.38	176.10
23	0.52	-5.75	28.20	1.78	5.00	-108.79	0.15	-16.51	-80.97	0.10	-19.69	163.29
24	0.52	-5.60	20.04	1.67	4.45	-118.23	0.15	-16.27	-85.94	0.13	-17.99	152.12
25	0.53	-5.44	11.74	1.58	3.95	-127.94	0.16	-15.93	-91.73	0.15	-16.23	141.89
26	0.54	-5.31	3.35	1.49	3.44	-137.60	0.17	-15.63	-97.31	0.18	-15.01	131.61
27	0.55	-5.25	-4.75	1.40	2.92	-147.29	0.17	-15.30	-103.67	0.21	-13.76	122.83
28	0.55	-5.18	-13.14	1.32	2.41	-156.96	0.18	-14.97	-110.73	0.23	-12.60	115.49
29	0.56	-5.10	-21.24	1.24	1.87	-166.74	0.19	-14.65	-117.22	0.25	-11.87	107.66
30	0.56	-4.97	-28.87	1.17	1.37	-176.51	0.19	-14.44	-125.53	0.27	-11.27	98.81
31	0.57	-4.86	-37.32	1.10	0.85	173.80	0.20	-14.07	-133.23	0.29	-10.66	91.12
32	0.58	-4.73	-45.58	1.04	0.33	163.80	0.20	-13.82	-141.57	0.31	-10.18	82.29
33	0.59	-4.57	-53.12	0.98	-0.20	153.80	0.21	-13.63	-150.48	0.32	-9.78	72.68
34	0.61	-4.32	-60.88	0.92	-0.73	143.95	0.22	-13.32	-159.58	0.34	-9.35	64.58
35	0.63	-4.08	-68.98	0.86	-1.32	133.28	0.22	-13.22	-169.26	0.35	-9.07	55.81
36	0.64	-3.86	-75.63	0.81	-1.87	123.11	0.22	-13.01	-179.29	0.37	-8.67	45.15

VMMK-2503 Application and Usage

(Please always refer to the latest Application Note AN5378 in website)

Biasing and Operation

The VMMK-2503 is normally biased with a positive drain supply connected to the output pin through an external bias-tee and with bypass capacitors as shown in Figure 19. The recommended drain supply voltage is 5 V and the corresponding drain current is approximately 65mA. The input of the VMMK-2503 is AC coupled and a DC-blocking capacitor is not required. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or low noise (Γopt) matching.

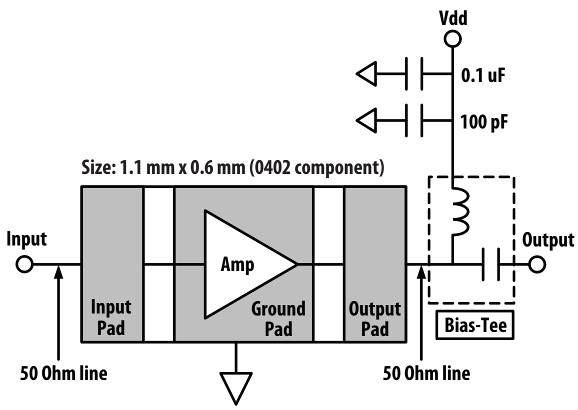


Figure 19. Usage of the VMMK-2503

Biasing the device at 5V compared to 4V results in higher gain, higher IP3 and P1dB. In a typical application, the bias-tee can be constructed using lumped elements. The value of the output inductor can have a major effect on both low and high frequency operation. The demo board uses an 10nH inductor that has self resonant frequency higher than the maximum desired frequency of operation. At frequencies higher than 6GHz, it may be advantageous to use a quarter-wave long micro-strip line to act as a high-impedance at the desired frequency of operation. This technique proves a good solution but only over relatively narrow bandwidths.

Another approach for broadbanding the VMMK-2503 is to series two different value inductors with the smaller value inductor placed closest to the device and favoring the higher frequencies. The larger value inductor will then offer better low frequency performance by not loading the output of the device. The parallel combination of the 100pF and 0.1uF capacitors provide a low impedance in the band of operation and at lower frequencies and should be placed as close as possible to the inductor. The low frequency bypass provides good rejection of power supply noise and also provides a low impedance termination for third order low frequency mixing products that will be generated when multiple in-band signals are injected into any amplifier.

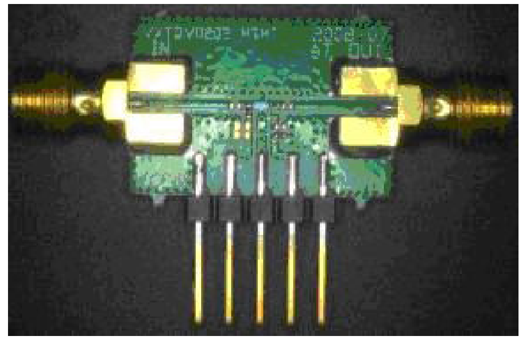


Figure 20. Evaluation/Test Board (available to qualified customer request)

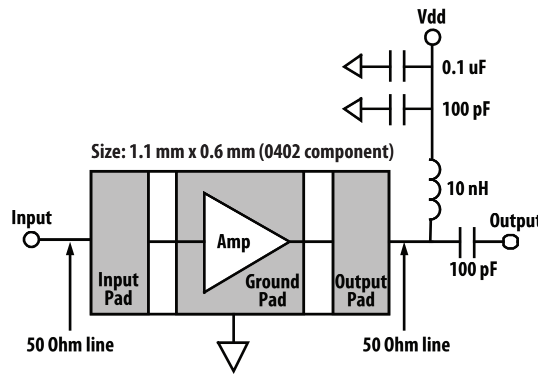


Figure 21. Example application of VMMK-2503 at 5.8GHz

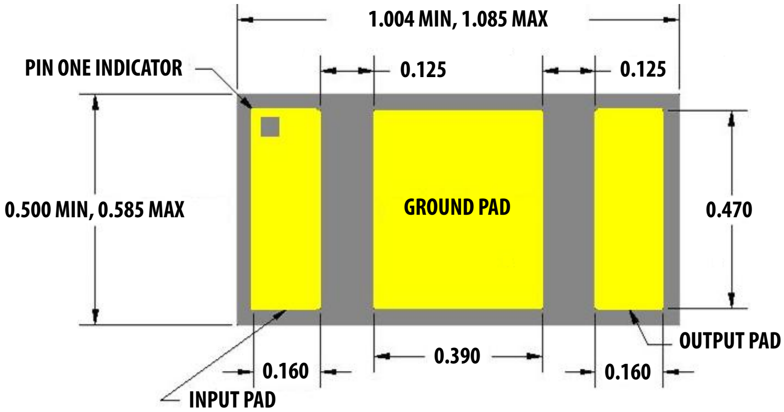
Refer the Absolute Maximum Ratings table for allowed DC and thermal conditions.

S Parameter Measurements

The S-parameters are measured on a .016 inch thick RO4003 printed circuit test board, using G-S-G (ground signal ground) probes. Coplanar waveguide is used to provide a smooth transition from the probes to the device under test. The presence of the ground plane on top of the test board results in excellent grounding at the device under test. A combination of SOLT (Short - Open - Load - Thru) and TRL (Thru - Reflect - Line) calibration techniques are used to correct for the effects of the test board, resulting in accurate device S-parameters. The reference plane for the S Parameters is at the edge of the package.

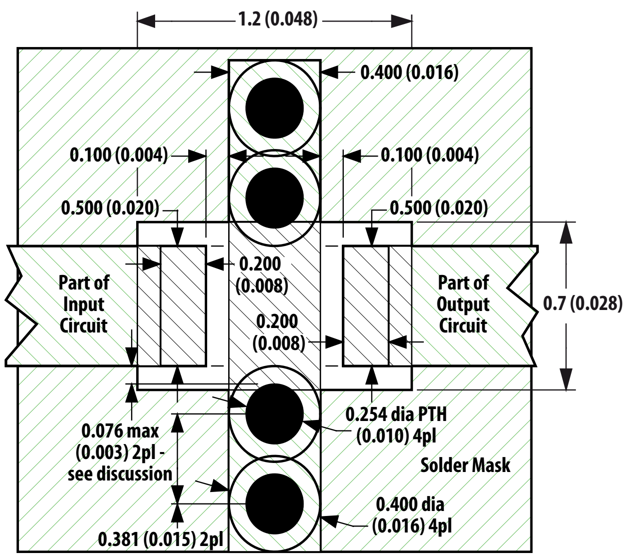
The product consistency distribution charts shown on page 2 represent data taken by the production wafer probe station using a 300um G-S wafer probe. The ground-signal probing that is used in production allows the device to be probed directly at the device with minimal common lead inductance to ground. Therefore there will be a slight difference in the nominal gain obtained at the test frequency using the 300um G-S wafer probe versus the 300um G-S-G printed circuit board substrate method.

Outline Drawing



Notes:
Solderable area of the device shown in yellow.
Dimensions in mm.
Tolerance ± 0.015 mm

Suggested PCB Material and Land Pattern



Notes:
1. 0.010" Rogers RO4350

Recommended SMT Attachment

The VMMK Packaged Devices are compatible with high volume surface mount PCB assembly processes.

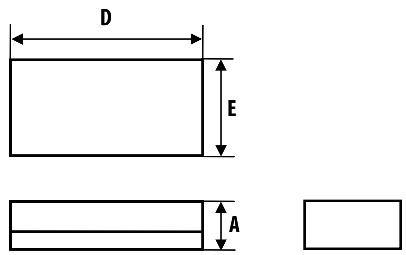
Manual Assembly for Prototypes

1. Follow ESD precautions while handling packages.
2. Handling should be along the edges with tweezers or from topside if using a vacuum collet.
3. Recommended attachment is solder paste. Please see recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
4. Apply solder paste using either a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance. **Excessive solder will degrade RF performance.**
5. Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp to avoid damage due to thermal shock.
6. Packages have been qualified to withstand a peak temperature of 260°C for 20 to 40 sec. Verify that the profile will not expose device beyond these limits.
7. Clean off flux per vendor's recommendations.
8. Clean the module with Acetone. Rinse with alcohol. Allow the module to dry before testing.

Ordering Information

Part Number	Devices Per Container	Container
VMMK-2503-BLKG	100	Antistatic Bag
VMMK-2503-TR1G	5000	7" Reel

Package Dimension Outline

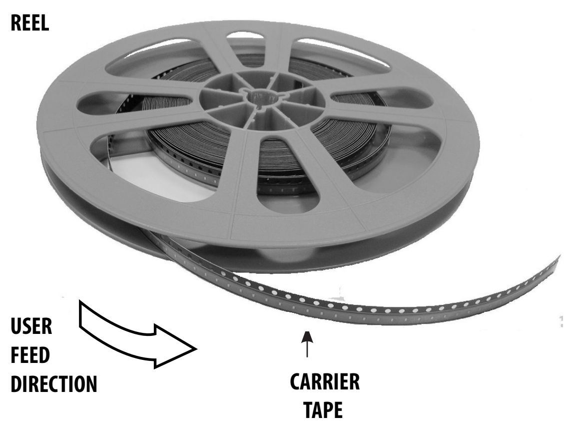


Die dimension:

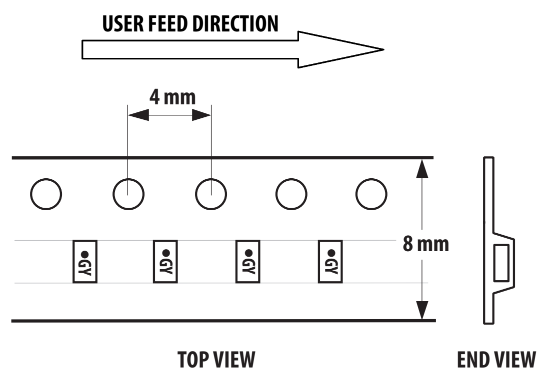
Dim	Range	Unit
D	1.004 - 1.085	mm
E	0.500 - 0.585	mm
A	0.225 - 0.275	mm

Note:
All dimensions are in mm

Reel Orientation

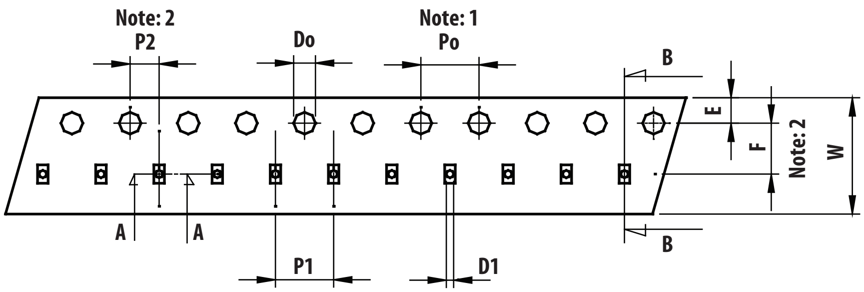


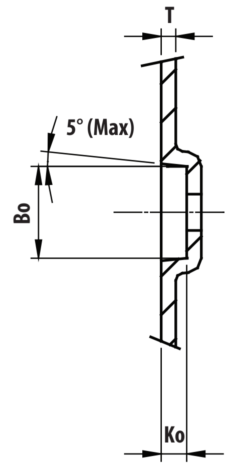
Device Orientation



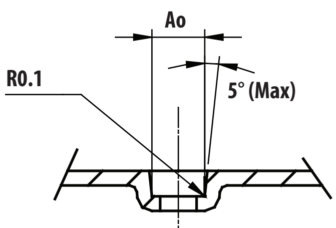
Note:
"G" = Device Code
"Y" = Month Code

Tape Dimensions





Scale 5:1
B–B SECTION



Scale 5:1
A–A SECTION

Ao = 0.73±0.05 mm

Bo = 1.26±0.05 mm

Ko = 0.35 $^{+0.05}_{+0}$ mm

Unit: mm

Symbol	Spec.
K1	–
Po	4.0±0.10
P1	4.0±0.10
P2	2.0±0.05
Do	1.55±0.05
D1	0.5±0.05
E	1.75±0.10
F	3.50±0.05
10Po	40.0±0.10
W	8.0±0.20
T	0.20±0.02

Notice:
1. 10 Sprocket hole pitch cumulative tolerance is ±0.1mm.
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a place 0.3mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1m per 100mm through a length of 250mm.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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