XA Spartan-7 Automotive FPGA Data Sheet: Overview

DS171 (v1.0) March 14, 2017 **Product Specification**

General Description

The Xilinx Automotive (XA) Spartan®-7 family of FPGAs, using the high-K metal gate (HKMG) process, provides the best combination of high performance and low power to service a wide variety of automotive applications. XA Spartan-7 FPGAs use the same 28HPL process as the established 7 series families and benefit from many of the same underlying architectural elements. The result is a family of compact, cost-optimized FPGAs that provide high logic and I/O performance with strictly controlled power consumption that are able to fit into aggressively small form factor packaging—all at a low cost.

The six-member family delivers expanded densities ranging from 6,000 to 102,400 logic cells and faster, more comprehensive connectivity. The XA Spartan-7 family offers a new, more efficient, dual-register 6-input look-up table (LUT) logic and a rich selection of built-in system-level blocks. These include 36Kb (2 x 18Kb) block RAMs with built-in FIFO logic for on-chip data buffering, DSP slices with 25 x 18 multiplier, 48-bit accumulator, and pre-adder for high-performance filtering, including optimized symmetric coefficient filtering, enhanced mixed-mode clock management blocks, SelectIO™ technology with support of DDR3 interfacing up to 800Mb/s, advanced system-level power management modes, auto-detect configuration options, and enhanced IP security with AES and Device DNA protection. These features provide a low-cost programmable alternative to custom ASIC products with unprecedented ease of use. XA Spartan-7 FPGAs offer the best solution for flexible and scalable high-volume logic designs, high-bandwidth parallel DSP processing designs, and cost-sensitive applications where multiple interfacing standards are required.

Summary of XA Spartan-7 FPGA Features

- Automotive Temperatures:
  - I-Grade: T_j = –40°C to +100°C
  - Q-Grade: T_j = –40°C to +125°C
- Automotive Standards:
  - Xilinx is ISO-TS16949 compliant
  - AEC-Q100 qualification
  - Production Part Approval Process (PPAP) documentation
  - Beyond AEC-Q100 qualification is available upon request
- Designed for low cost
  - Multiple efficient integrated blocks
  - Optimized selection of I/O standards
  - High-volume plastic wire-bonded packages
- Low static and dynamic power
  - 28 nm process optimized for cost and low power
- High-performance SelectIO technology with support for DDR3
  - Up to 1250 Mb/s data transfer rate per differential I/O
  - Selectable output drive, up to 24mA per pin
  - 3.3V to 1.2V I/O standards and protocols
  - Low-cost HSTL and SSTL memory interfaces
  - Adjustable I/O slew rates to improve signal integrity
- Efficient DSP slices
  - High-performance arithmetic and signal processing
  - Fast 25 x 18 multiplier and 48-bit accumulator
  - Pipelining and cascading capability
  - Pre-adder to assist filter applications
- Integrated Memory Controller blocks
  - DDR, DDR2, DDR3, and LPDDR support
  - Data rates up to 800Mb/s
  - Multi-port bus structure with independent FIFO to reduce design timing issues
- Abundant logic resources with increased logic capacity
  - Optional shift register or distributed RAM support
  - Efficient 6-input LUTs improve performance and minimize power
  - LUT with dual flip-flops for pipeline centric applications
- Block RAM with a wide range of granularity
  - Fast block RAM with byte write enable
  - 36Kb blocks that can be optionally programmed as two independent 18Kb block RAMs
- Clock Management Tile (CMT) for enhanced performance
  - Low noise, flexible clocking
  - Digital Clock Managers (DCMs) eliminate clock skew and duty cycle distortion
  - Phase-Locked Loops (PLLs) for low-jitter clocking
  - Frequency synthesis with simultaneous multiplication, division, and phase shifting
  - 32 low-skew global clock networks
- Simplified configuration supports low-cost standards:
  - 2-pin auto-detect configuration
  - Broad third-party SPI (up to x4) flash support
  - Multi-boot support for remote upgrade with multiple bitstreams, using watchdog protection
- Enhanced security for design protection.
  - Unique Device DNA identifier for design authentication
- Wide variety of configuration options, including support for commodity memories, 256-bit AES encryption with HMAC/SHA-256 authentication, and built-in SEU detection and correction
- Industry-leading IP and reference designs
- Strong automotive-specific third-party ecosystem with IP, development boards, and design services

XA Spartan-7 FPGA Feature Summary

Table 1: **XA Spartan-7 FPGA Feature Summary by Device**

Device	Logic Cells	CLB		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe	GT	XADC Blocks	Total I/O Banks[5]	Max User I/O
		Slices[1]	Max Distributed RAM (Kb)		18Kb	36Kb	Max (Kb)						
XA7S6	6,000	938	70	10	10	5	180	2	0	0	0	2	100
XA7S15	12,800	2,000	150	20	20	10	360	2	0	0	0	2	100
XA7S25	23,360	3,650	313	80	90	45	1,620	3	0	0	1	3	150
XA7S50	52,160	8,150	600	120	150	75	2,700	5	0	0	1	5	250
XA7S75	76,800	12,000	832	140	180	90	3,240	8	0	0	1	8	400
XA7S100	102,400	16,000	1,110	160	240	120	4,320	8	0	0	1	8	400

Notes:

1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Does not include configuration Bank 0.

FPGA Device Package Combinations and Available I/Os

Table 2: **XA Spartan-7 FPGA Device-Package Combinations and Maximum I/Os**

Package	CPGA196	CSGA225	CSGA324	FTGB196	FGGA484	FGGA676
Size (mm)	8 x 8	13 x 13	15 x 15	15 x 15	23 x 23	27 x 27
Ball Pitch (mm)	0.5	0.8	0.8	1.0	1.0	1.0
Device	HR I/O[1]	HR I/O[1]	HR I/O[1]	HR I/O[1]	HR I/O[1]	HR I/O[1]
XA7S6	100	100		100		
XA7S15	100	100		100		
XA7S25		150	150	100		
XA7S50			210	100	250	
XA7S75					338	400
XA7S100					338	400

Notes:

1. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

CLBs, Slices, and LUTs

Some key features of the CLB architecture include:

- Real 6-input look-up tables (LUTs)
- Memory capability within the LUT
- Register and shift register functionality

The LUTs in XA Spartan-7 FPGAs can be configured as either one 6-input LUT (64-bit ROMs) with one output, or as two 5-input LUTs (32-bit ROMs) with separate outputs but common addresses or logic inputs. Each LUT output can optionally be registered in a flip-flop. Four such LUTs and their eight flip-flops as well as multiplexers and arithmetic carry logic form a slice, and two slices form a configurable logic block (CLB). Four of the eight flip-flops per slice (one per LUT) can optionally be configured as latches.

Between 25–50% of all slices can also use their LUTs as distributed 64-bit RAM or as 32-bit shift registers (SRL32) or as two SRL16s. Modern synthesis tools take advantage of these highly efficient logic, arithmetic, and memory features.

Clock Management

Some of the key highlights of the clock management architecture include:

- High-speed buffers and routing for low-skew clock distribution
- Frequency synthesis and phase shifting
- Low-jitter clock generation and jitter filtering

Each XA Spartan-7 FPGA has up to 8 clock management tiles (CMTs), each consisting of one mixed-mode clock manager (MMCM) and one phase-locked loop (PLL).

Mixed-Mode Clock Manager and Phase-Locked Loop

The MMCM and PLL share many characteristics. Both can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of both components is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers: D, M, and O. The pre-divider D (programmable by configuration and afterwards via DRP) reduces the input frequency and feeds one input of the traditional PLL phase/frequency comparator. The feedback divider M (programmable by configuration and afterwards via DRP) acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each can be selected to drive one of the output dividers (six for the PLL, O0 to O5, and seven for the MMCM, O0 to O6), each programmable by configuration to divide by any integer from 1 to 128.

The MMCM and PLL have three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-bandwidth mode has the best jitter attenuation but not the smallest phase offset. High-bandwidth mode has the best phase offset, but not the best jitter attenuation. Optimized mode allows the tools to find the best setting.

MMCM Additional Programmable Features

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of $^1/_8$ and can thus increase frequency synthesis capabilities by a factor of 8.

The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,440MHz, the phase-shift timing increment is 13ps.

Clock Distribution

Each XA Spartan-7 FPGA provides six different types of clock lines (BUFG, BUFR, BUFIO, BUFH, BUFMR, and the high-performance clock) to address the different clocking requirements of high fanout, short propagation delay, and extremely low skew.

Global Clock Lines

In each XA Spartan-7 FPGA (except XA7S6 and XA7S15), 32 global clock lines have the highest fanout and can reach every flip-flop clock, clock enable, and set/reset, as well as many logic inputs. There are 12 global clock lines within any clock region driven by the horizontal clock buffers (BUFH). Each BUFH can be independently enabled/disabled, allowing for clocks to be turned off within a region, thereby offering fine-grain control over which clock regions consume power. Global clock lines can be driven by global clock buffers, which can also perform glitchless clock multiplexing and clock enable functions. Global clocks are often driven from the CMT, which can completely eliminate the basic clock distribution delay.

Regional Clocks

Regional clocks can drive all clock destinations in their region. A region is defined as an area that is 50 I/O and 50 CLB high and half the chip wide. XA Spartan-7 FPGAs have between two and eight regions. There are four regional clock tracks in every region. Each regional clock buffer can be driven from any of four clock-capable input pins, and its frequency can optionally be divided by any integer from 1 to 8.

I/O Clocks

I/O clocks are especially fast and serve only I/O logic and serializer/deserializer (SerDes) circuits, as described in the I/O Logic section. The XA Spartan-7 devices have a direct connection from the MMCM to the I/O for low-jitter, high-performance interfaces.

Block RAM

Some of the key features of the block RAM include:

- Dual-port 36Kb block RAM with port widths of up to 72
- Programmable FIFO logic
- Built-in optional error correction circuitry

Every XA Spartan-7 FPGA has between 5 and 120 dual-port block RAMs, each storing 36Kb. Each block RAM has two completely independent ports that share nothing but the stored data.

Synchronous Operation

Each memory access, read or write, is controlled by the clock. All inputs, data, address, clock enables, and write enables are registered. Nothing happens without a clock. The input address is always clocked, retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency.

During a write operation, the data output can reflect either the previously stored data, the newly written data, or can remain unchanged.

Programmable Data Width

Each port can be configured as 32K × 1, 16K × 2, 8K × 4, 4K × 9 (or 8), 2K × 18 (or 16), 1K × 36 (or 32), or 512 × 72 (or 64). The two ports can have different aspect ratios without any constraints.

Each block RAM can be divided into two completely independent 18Kb block RAMs that can each be configured to any aspect ratio from 16K × 1 to 512 × 36. Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs.

Only in simple dual-port (SDP) mode can data widths of greater than 18 bits (18Kb RAM) or 36 bits (36Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72.

Both sides of the dual-port 36Kb RAM can be of variable width.

Two adjacent 36Kb block RAMs can be configured as one cascaded 64K × 1 dual-port RAM without any additional logic.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multi-rate) operation increments the internal addresses and provides four handshaking flags: full, empty, almost full, and almost empty. The almost full and almost empty flags are freely programmable. Similar to the block RAM, the FIFO width and depth are programmable, but the write and read ports always have identical width.

First word fall-through mode presents the first-written word on the data output even before the first read operation. After the first word has been read, there is no difference between this mode and the standard mode.

Digital Signal Processing — DSP Slice

Some highlights of the DSP functionality include:

- 25 × 18 twos complement multiplier/accumulator high-resolution (48 bit) signal processor
- Power saving pre-adder to optimize symmetrical filter applications
- Advanced features: optional pipelining, optional ALU, and dedicated buses for cascading

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All 7 series FPGAs have many dedicated, full custom, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 25 × 18 bit two's complement multiplier and a 48-bit accumulator, both capable of operating up to 550MHz. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The DSP also includes a 48-bit-wide Pattern Detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

Input/Output

Some highlights of the input/output functionality include:

- High-performance SelectIO technology with support for 800Mb/s DDR3
- Digitally Controlled Impedance that can be 3-stated for lowest power, high-speed I/O operation

The number of I/O pins varies depending on device and package size. Each I/O is configurable and can comply with a large number of I/O standards. With the exception of the supply pins and a few dedicated configuration pins, all other package pins have the same I/O capabilities, constrained only by certain banking rules. The I/O in XA Spartan-7 FPGAs are classed as high range (HR). HR I/Os offer a wide range of voltage support, from 1.2V to 3.3V.

HR I/O pins in XA Spartan-7 FPGAs are organized in banks, with 50 pins per bank. Each bank has one common V_{CCO} output supply, which also powers certain input buffers. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). There are two V_{REF} pins per bank (except configuration bank 0). A single bank can have only one V_{REF} voltage value.

XA Spartan-7 FPGAs use small form factor wire-bond packages for lowest cost.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All XA Spartan-7 devices support differential standards beyond LVDS: RSDS, BLVDS, differential SSTL, and differential HSTL.

Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended SSTL and differential SSTL. The SSTL I/O standard can support data rates of up to 800Mb/s for DDR3 interfacing applications.

Low Power I/O Features

The I/Os have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input Delay

All inputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input can be individually delayed by up to 32 increments of 78ps, 52ps, or 39ps each. Such delays are implemented as IDELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O structure. Each I/O pin possesses an 8-bit IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 3, 4, 5, 6, 7, or 8 bits. By cascading two IOSERDES from two adjacent pins (default from differential I/O), wider width conversions of 10 and 14 bits can also be supported. The ISERDES has a special oversampling mode capable of asynchronous data recovery for applications like a 1.25Gb/s LVDS I/O-based SGMII interface.

Configuration

There are many advanced configuration features, including:

- High-speed SPI configuration
- Built-in multi-boot and safe-update capability
- 256-bit AES encryption with HMAC/SHA-256 authentication
- Built-in SEU detection and correction
- Partial reconfiguration

XA Spartan-7 FPGAs store their customized configuration in SRAM-type internal latches. There are up to 30Mb configuration bits, depending on device size and user-design implementation options. The configuration storage is volatile and must be reloaded whenever the FPGA is powered up. This storage can also be reloaded at any time by pulling the PROGRAM_B pin Low. Several methods and data formats for loading configuration are available, determined by the three mode pins.

The SPI interface (x1, x2, and x4 modes) is a common method used for configuring the FPGA. Users can directly connect an SPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, and x4 for SPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on. Refer to UG470, *7 Series FPGAs Configuration User Guide* for details.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide are also supported by the FPGA that are especially useful for processor-driven configuration.

The FPGA has the ability to reconfigure itself with a different image using SPI flash, eliminating the need for an external controller. The FPGA can reload its original design in case there are any errors in the data transmission, ensuring an operational FPGA at the end of the process. This is especially useful for updates to a design after the end product has been shipped. Customers can ship their products with an early version of the design, thus getting their products to market faster. This feature allows customers to keep their end users current with the most up-to-date designs while the product is already in the field.

The dynamic reconfiguration port (DRP) gives the system designer easy access to the configuration and status registers of the MMCM, PLL, and XADC. The DRP behaves like a set of memory-mapped registers, accessing and modifying block-specific configuration bits as well as status and control registers.

Encryption, Readback, and Partial Reconfiguration

In all 7 series FPGAs (except XA7S6 and XA7S15), the FPGA bitstream, which contains sensitive customer IP, can be protected with 256-bit AES encryption and HMAC/SHA-256 authentication to prevent unauthorized copying of the design. The FPGA performs decryption on the fly during configuration using an internally stored 256-bit key. This key can reside in battery-backed RAM or in nonvolatile eFUSE bits.

Most configuration data can be read back without affecting the system's operation. Typically, configuration is an all-or-nothing operation, but XA Spartan-7 support partial reconfiguration. This is an extremely powerful and flexible feature that allows the user to change portions of the FPGA while other portions remain static. Users can time-slice these portions to fit more IP into smaller devices, saving cost and power. Where applicable in certain designs, partial reconfiguration can greatly improve the versatility of the FPGA.

XADC (Analog-to-Digital Converter)

Highlights of the XADC architecture include:

- Dual 12-bit 1 MSPS analog-to-digital converters (ADCs)
- Up to 17 flexible and user-configurable analog inputs
- On-chip or external reference option
- On-chip temperature (±4°C max error) and power supply (±1% max error) sensors
- Continuous JTAG access to ADC measurements

All Xilinx 7 series FPGAs (except XA7S6 and XA7S15) integrate a new flexible analog interface called XADC. When combined with the programmable logic capability of the 7 series FPGAs, the XADC can address a broad range of data acquisition and monitoring requirements. For more information, go to: http://www.xilinx.com/ams.

The XADC contains two 12-bit 1 MSPS ADCs with separate track and hold amplifiers, an on-chip analog multiplexer (up to 17 external analog input channels supported), and on-chip thermal and supply sensors. The two ADCs can be configured to simultaneously sample two external-input analog channels. The track and hold amplifiers support a range of analog input signal types, including unipolar, bipolar, and differential. The analog inputs can support signal bandwidths of at least 500KHz at sample rates of 1 MSPS. It is possible to support higher analog bandwidths using external analog multiplexer mode with the dedicated analog input (see UG480, *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide*).

The XADC optionally uses an on-chip reference circuit (±1%), thereby eliminating the need for any external active components for basic on-chip monitoring of temperature and power supply rails. To achieve the full 12-bit performance of the ADCs, an external 1.25V reference IC is recommended.

If the XADC is not instantiated in a design, then by default it digitizes the output of all on-chip sensors. The most recent measurement results (together with maximum and minimum readings) are stored in dedicated registers for access at any time via the JTAG interface. User-defined alarm thresholds can automatically indicate over-temperature events and unacceptable power supply variation. A user-specified limit (for example, 100°C) can be used to initiate an automatic powerdown.

XA Spartan-7 FPGA Ordering Information

Table 3 shows the speed and temperature grades available for the XA Spartan-7 FPGAs. Some devices might not be available in every speed and temperature grade.

Table 3: **XA Spartan-7 FPGA Speed Grade and Temperature Ranges**

Device Family	Devices	Speed Grade, Temperature Range, and Operating Voltage	
		Industrial (I) –40°C to +100°C	**Automotive (Q) –40°C to +125°C**
XA Spartan-7	All	-2I (1.0V)	
		-1I (1.0V)	-1Q (1.0V)

The XA Spartan-7 FPGA ordering information is shown in Figure 1. Refer to the Package Marking section of UG475, *7 Series FPGAs Packaging and Pinout* for a more detailed explanation of the device markings.

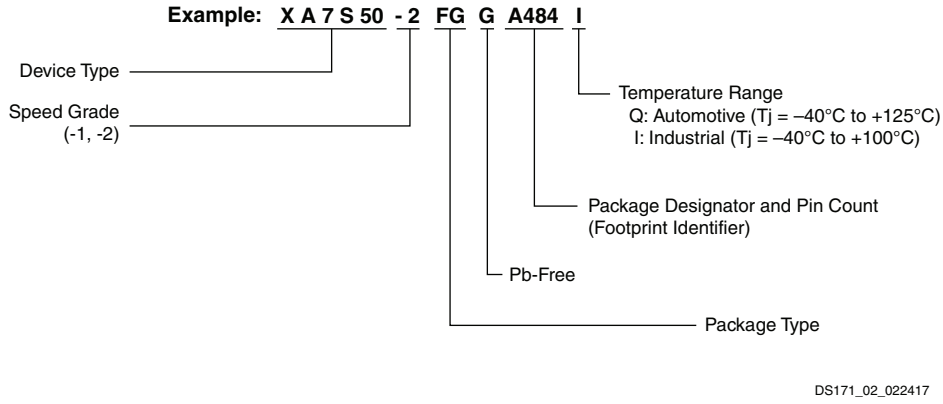

Figure 1: **XA Spartan-7 FPGA Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/14/2017	1.0	Initial Xilinx release.

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