

## N-channel 100 V, 3.9 mΩ typ., 180 A, STripFET™ F3 Power MOSFET in H<sup>2</sup>PAK-6 package

Datasheet - production data

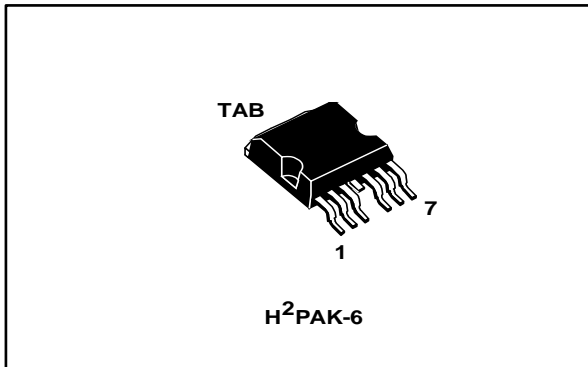
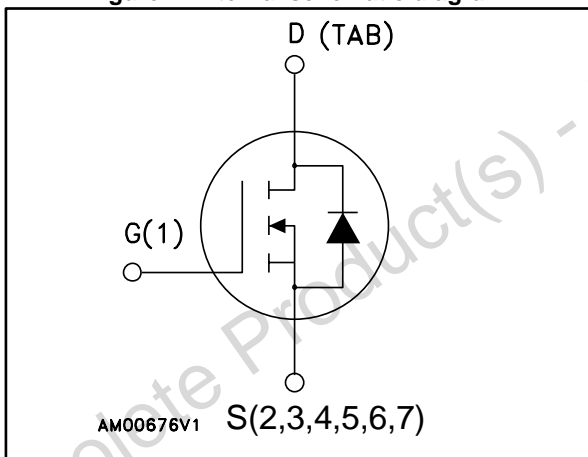


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STH180N10F3-6	100 V	4.5 mΩ	180 A

- Low on-resistance R<sub>DS(on)</sub>
- 100% avalanche tested

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1: Device summary

Order code	Marking	Package	Packing
STH180N10F3-6	180N10F3	H <sup>2</sup> PAK-6	Tape and reel

---

**Contents**

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.1 Electrical characteristics (curves).....	6
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package information .....</b>	<b>9</b>
	4.1 H <sup>2</sup> PAK-6 package information.....	9
	4.2 Packing information.....	12
<b>5</b>	<b>Revision history .....</b>	<b>14</b>

Obsolete Product(s) - Obsolete Product(s)

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	315	W
	Derating factor	2.1	W/°C
dv/dt	Peak diode recovery voltage slope	20	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	350	mJ
$T_J$	Operating junction temperature	-55 to 175	°C
$T_{stg}$	Storage temperature		°C

**Notes:**

- (1) Current limited by package
- (2) Pulse width limited by safe operating area
- (3) Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 80$ ,  $V_{DD} = 50\text{ V}$

**Table 3: Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.48	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	°C/W

**Notes:**

- (1) When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4: On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 250\ \mu A$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 100\ V$			10	$\mu A$
		$V_{DS} = 100\ V$ ; $T_C = 125\text{ °C}$			100	$\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\ V$			$\pm 200$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ V$ , $I_D = 60\ A$		3.9	4.5	m $\Omega$

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$C_{iss}$	Input capacitance	$V_{DS} = 25\ V$ , $f = 1\ MHz$ , $V_{GS} = 0$	-	6665	-	pF	
$C_{oss}$	Output capacitance			786		pF	
$C_{rss}$	Reverse transfer capacitance			49		pF	
$Q_g$	Total gate charge			$V_{DD} = 50\ V$ , $I_D = 120\ A$		114.6	nC
$Q_{gs}$	Gate-source charge			$V_{GS} = 10\ V$		38.8	nC
$Q_{gd}$	Gate-drain charge			See <a href="#">Figure 14: "Gate charge test circuit"</a>		31.9	nC

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ V$ , $I_D = 60\ A$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\ V$ See <a href="#">Figure 13: "Switching times test circuit for resistive load"</a>	-	25.6	-	ns
$t_r$	Rise time			97.1		ns
$t_{d(off)}$	Turn-off delay time			99.9		ns
$t_f$	Fall time			6.9		ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$I_{SD}$	Source-drain current		-		180	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				720	A	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 120 \text{ A}, V_{GS} = 0$				1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 120 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 80 \text{ V}, T_j = 150$ $^{\circ}\text{C}$			83.4		ns
$Q_{rr}$	Reverse recovery charge				295.7		nC
$I_{RRM}$	Reverse recovery current					7.1	

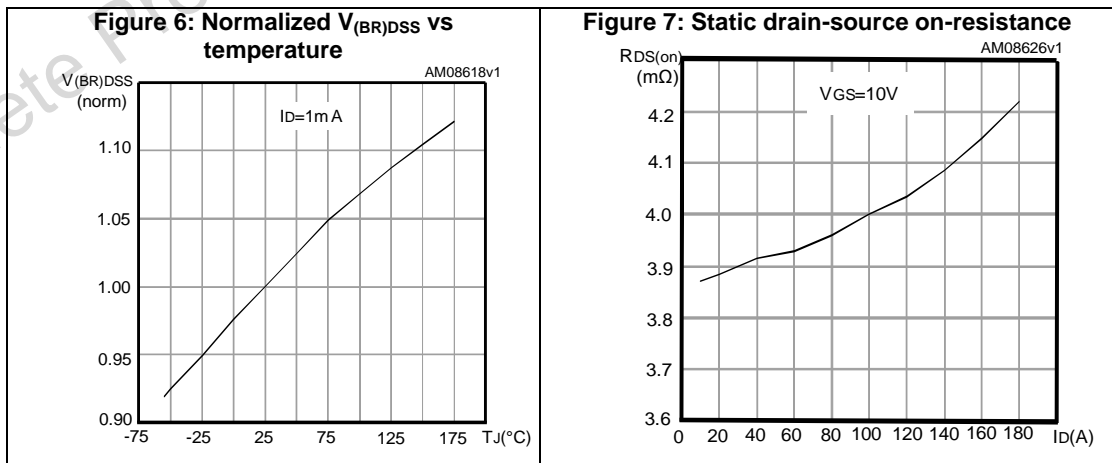
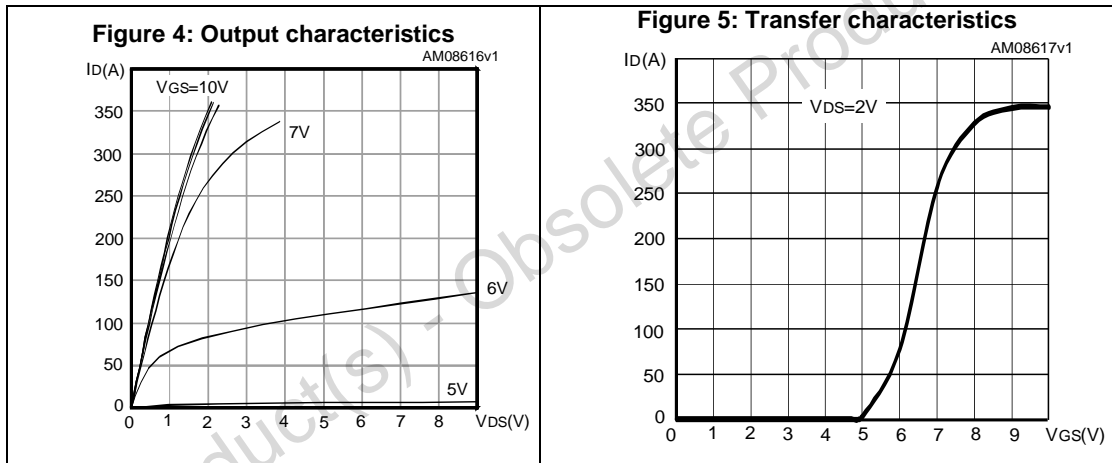
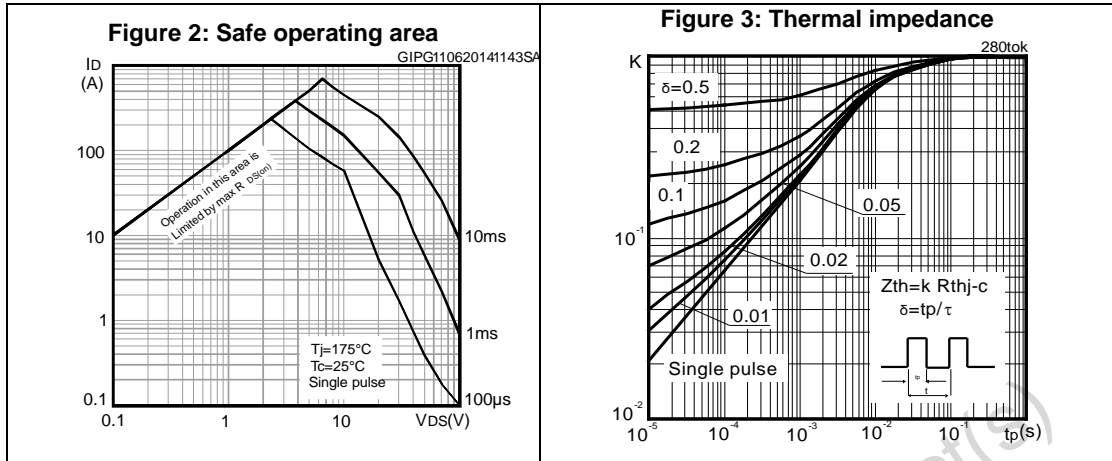
**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area

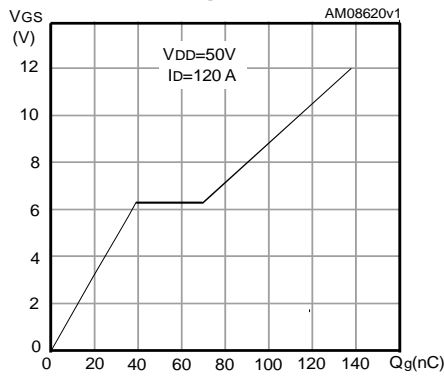
<sup>(2)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

Obsolete Product(s) - Obsolete Product(s)

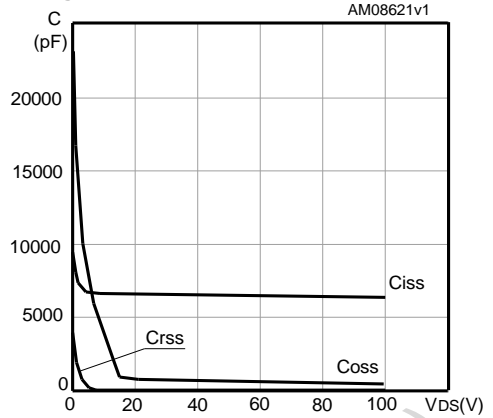
## 2.1 Electrical characteristics (curves)



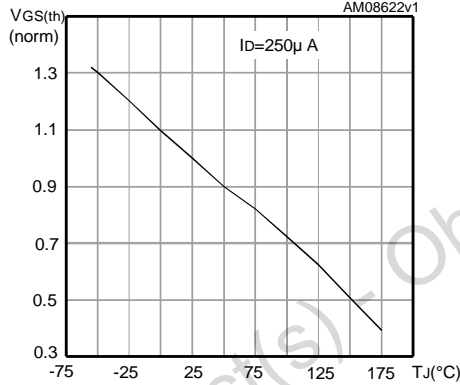
**Figure 8: Gate charge vs gate-source voltage**



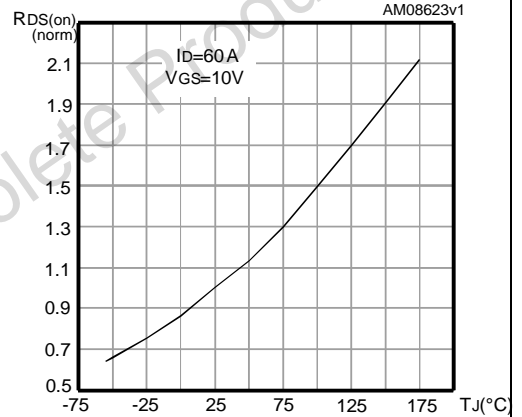
**Figure 9: Capacitance variations**



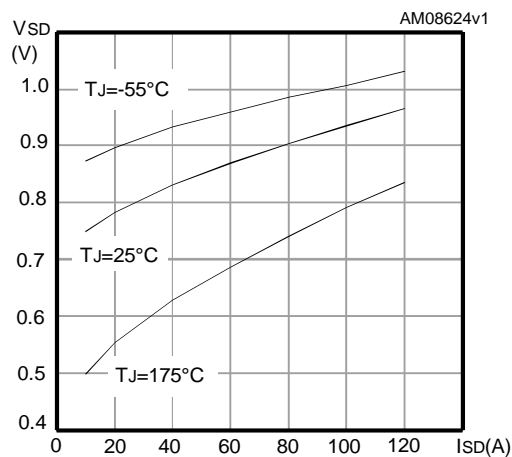
**Figure 10: Normalized gate threshold voltage vs temperature**



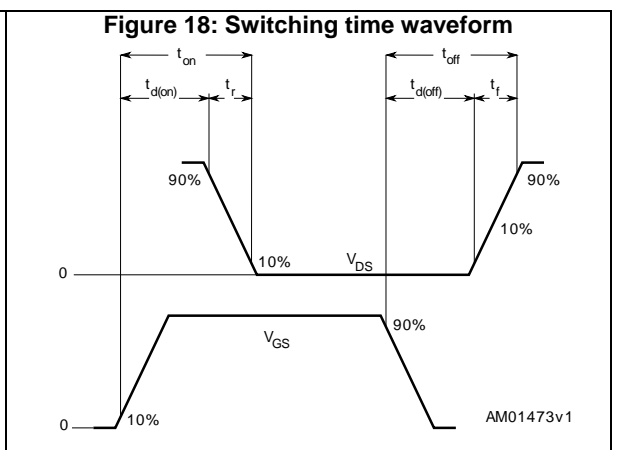
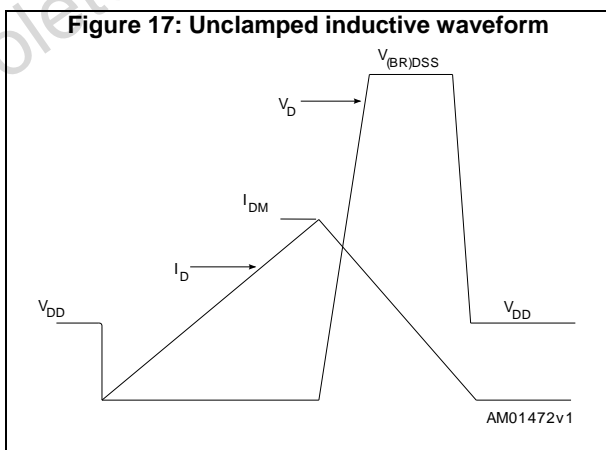
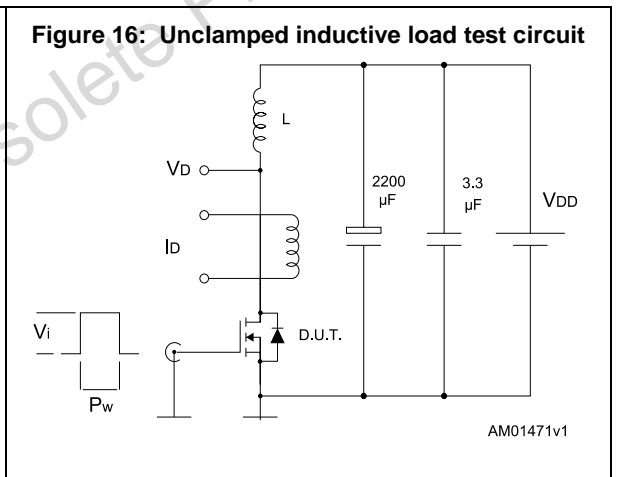
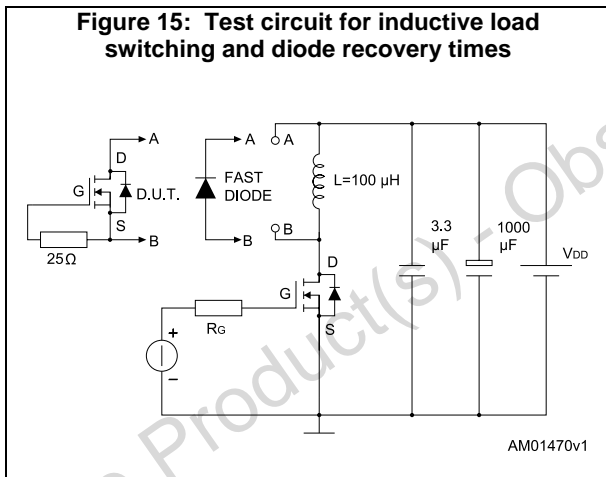
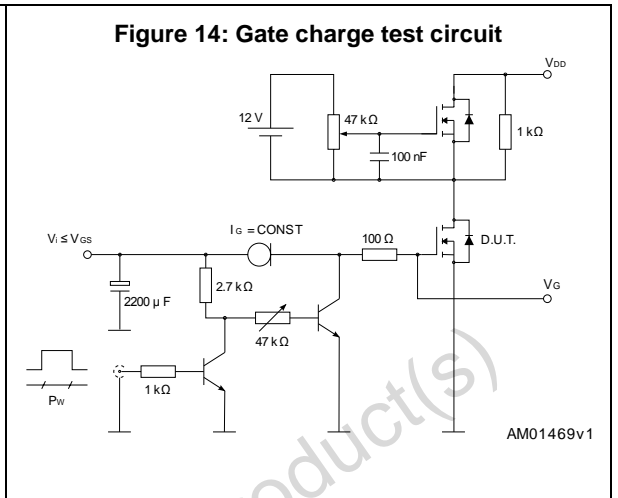
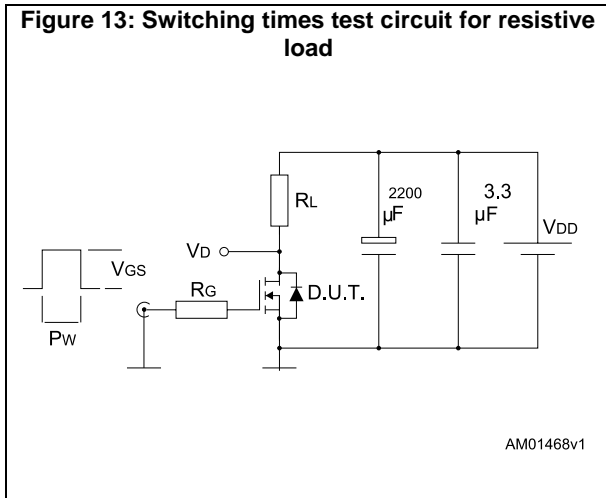
**Figure 11: Normalized on-resistance vs temperature**



**Figure 12: Source-drain diode forward characteristics**



### 3 Test circuits





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 H<sup>2</sup>PAK-6 package information

Figure 19: H<sup>2</sup>PAK-6 outline

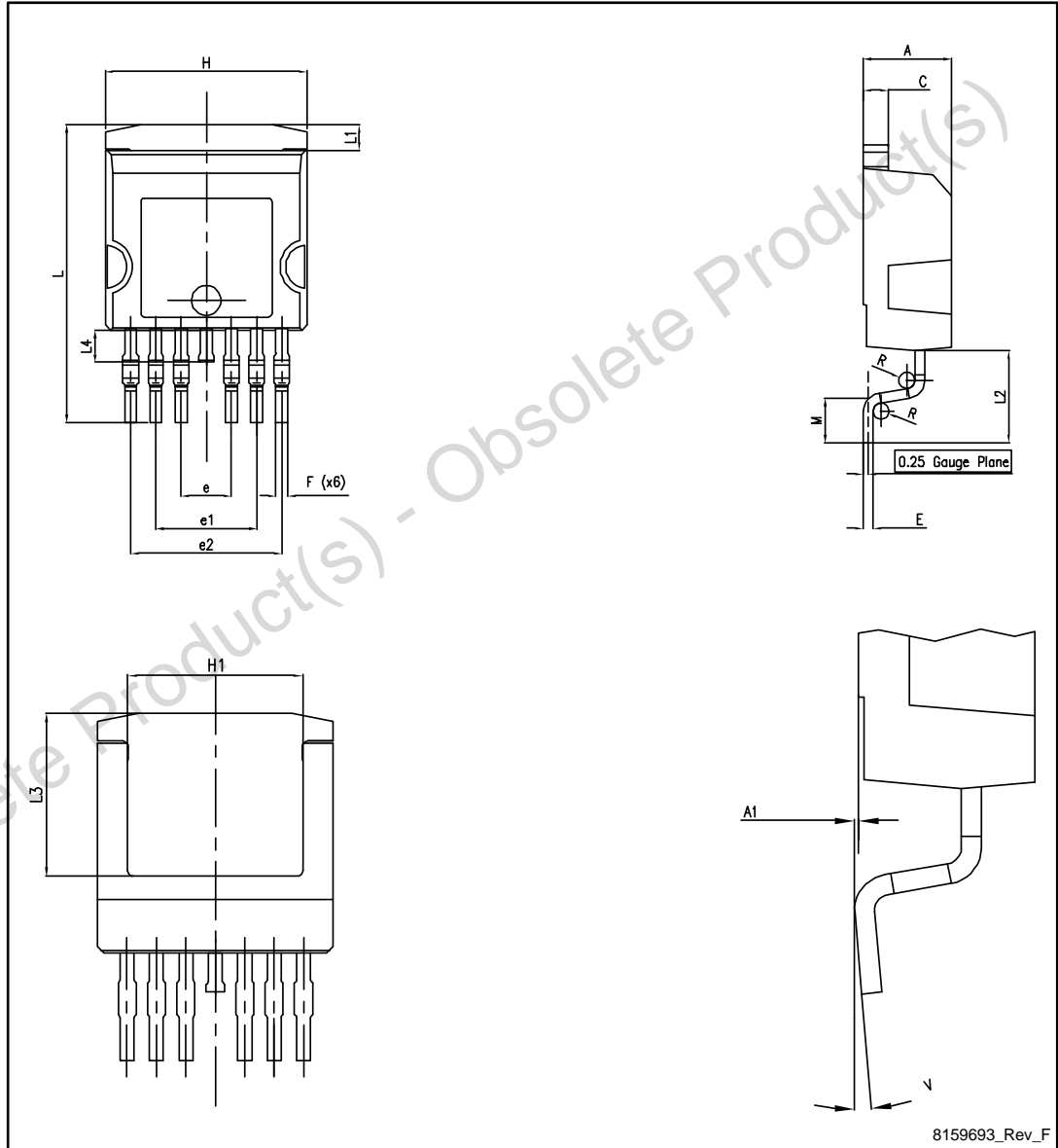
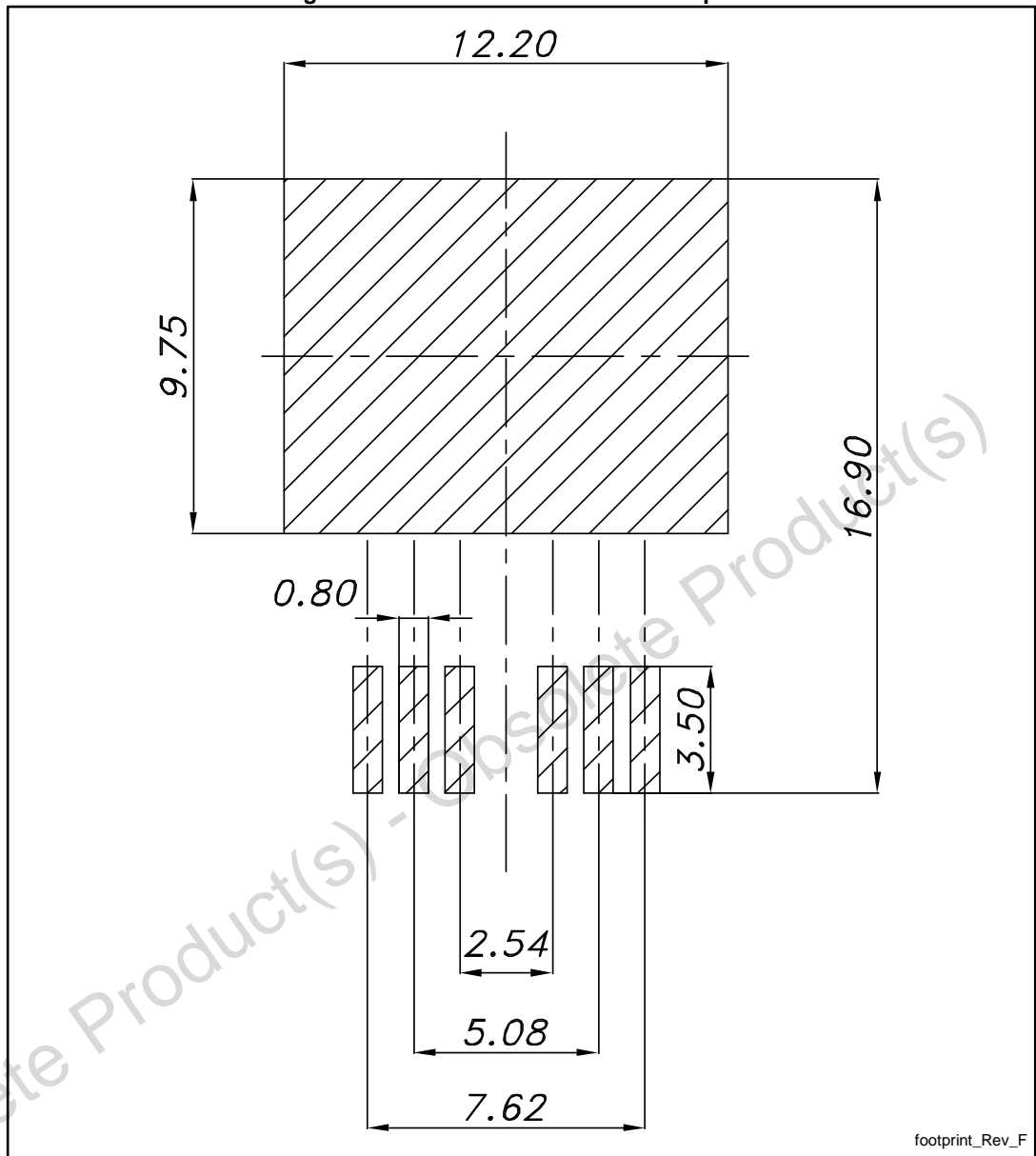


Table 8: H<sup>2</sup>PAK-6 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 20: H<sup>2</sup>PAK-6 recommended footprint



footprint\_Rev\_F



Dimensions are in mm.

### 4.2 Packing information

Figure 21: Tape outline

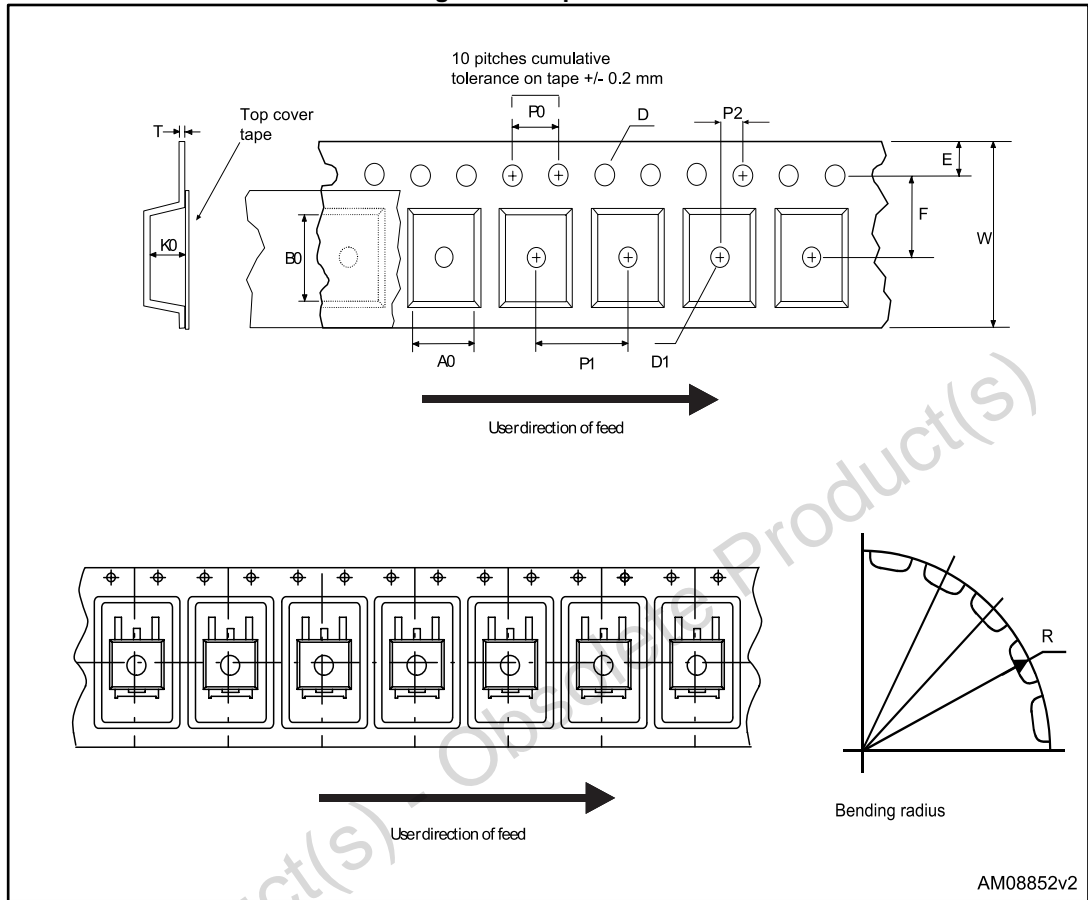


Figure 22: Reel outline

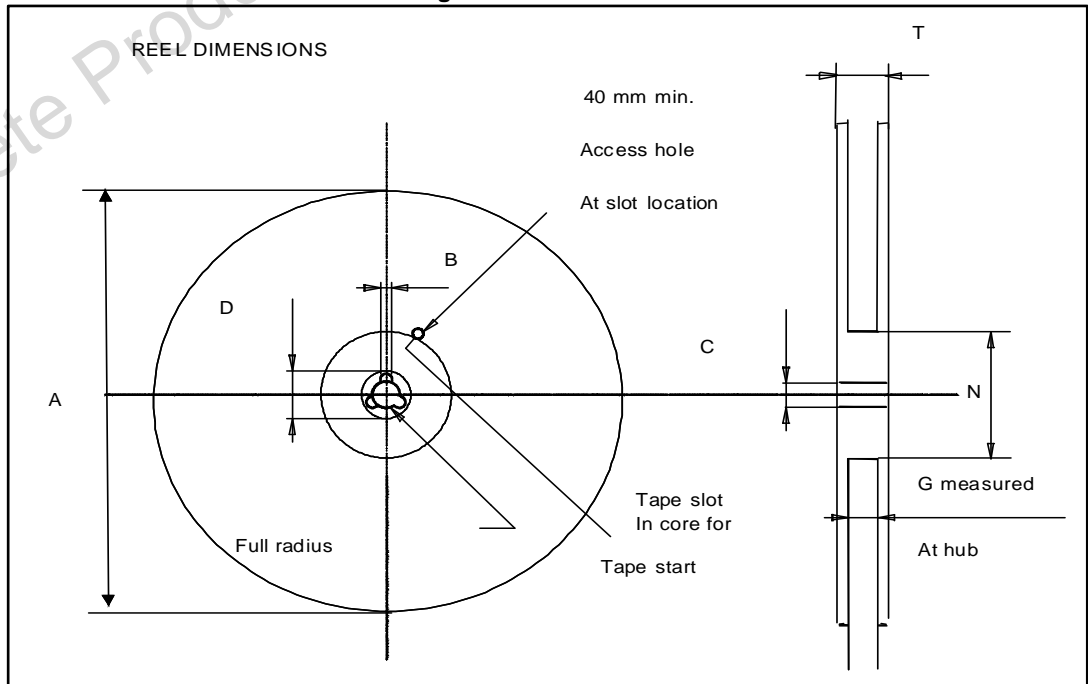


Table 9: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Obsolete Product(s) - Obsolete Product(s)

## 5 Revision history

**Table 10: Document revision history**

Date	Revision	Changes
10-Oct-2011	1	First version
04-Nov-2011	2	<ul style="list-style-type: none"><li>Updated features in cover page</li></ul>
14-Nov-2014	3	<ul style="list-style-type: none"><li>Updated: H<sup>2</sup>PAK-6 package mechanical data.</li><li>Updated: title, features and description.</li><li>Minor text changes.</li></ul>
26-Nov-2014	4	Updated <a href="#">Table 4: "On/off-state"</a> .

Obsolete Product(s) - Obsolete Product(s)

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved