PIC18F2220/2320/4220/4320 Rev. B2 Silicon Errata

The PIC18F2220/2320/4220/4320 Rev. B2 parts you have received conform functionally to the Device Data Sheet (DS39599**F**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC18F2220/2320/4220/4320 silicon.

The following silicon errata apply only to PIC18F2220/2320/4220/4320 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2220	0000 0101 100	0 0011
PIC18F2320	0000 0101 000	0 0011
PIC18F4220	0000 0101 101	0 0011
PIC18F4320	0000 0101 001	0 0011

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

1. Module: Internal Oscillator Block

If the INTRC clock source was not started at POR (any VDD) and VDD is greater than 4.5V, the INTRC clock source may not start or may require a long delay when starting. The INTRC may not restart when VDD is lowered below 4.5V.

Features that depend on the operation of the INTRC clock source may be affected. These include the INTOSC output when exiting from Sleep mode, the Watchdog Timer (WDT) if enabled by firmware using the WDTCON register, Two-Speed Start-ups during Reset or wake-up from Sleep and the Fail-Safe Clock Monitor (FSCM) when exiting Sleep mode.

The INTOSC frequency may rise very high (for example, 9.5 MHz). The WDT and the FSCM may simply not function. Two-Speed Start-ups may not occur, but execution will start once the primary clock source becomes ready.

Work around

Several work arounds may be used.

1. Enable the WDT in Configuration register, CONFIG2H and place a `CLRWDT` instruction somewhere in the main loop.
2. Configure the internal oscillator block as the primary clock source using Configuration Register 1H.
3. Any technique that starts the INTRC at Reset and does not disable it may be used.
4. Ensure that VDD is below 4.5V when starting the INTRC clock source.

There may be other work arounds.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Core (`DAW` Instruction)

The `DAW` instruction may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the `DAW` instruction. If the Carry bit is set, increment the next higher byte to be added, using an instruction such as `INCFSZ` (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the `DAW` instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80        ; .80 (BCD)
ADDLW   0x80        ; .80 (BCD)

BTFSC   STATUS,C    ; test C
INCFSZ  byte2       ; inc next higher LSB
DAW
BTFSC   STATUS,C    ; test C
INCFSZ  byte2       ; inc next higher LSB

This is repeated for each DAW instruction.
```

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Internal Oscillator Block

At high temperature (above 85°C) or low VDD (below 2.5V), the IOFS bit (OSCCON<2>) may not become set when the internal oscillator block is selected as the system clock source for any frequency above 31 kHz (OSCCON<6:4> ≠ 000). The INTOSC output will stabilize at 8 MHz; however, the IOFS bit may not become set.

Work around

If time critical code is to be executed, it should be delayed by 1 ms following the operation that enables the 8 MHz INTOSC output from the internal oscillator block.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: INTOSC

Incrementing or decrementing the value in the OSCTUNE register may not have the expected effect of shifting the INTRC or INTOSC output frequencies. The OSCTUNE values beyond which this happens may vary with temperatures above 70°C.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: MSSP (All I²C™ and SPI Modes)

The Buffer Full flag bit (BF) of the SSPSTAT register (SSPSTAT<0>) may be inadvertently cleared, even when the SSPBUF register has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = 1111) and
- Any instruction that contains C9h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

Identified work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh.

In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the Access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select all GPR Banks.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain C9h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: MSSP (SPI, Slave Mode)

In its current implementation, the $\overline{SS}$ (Slave Select) control signal generated by an external master processor may not be successfully recognized by the PIC® microcontroller operating in Slave Select mode (SSPM3:SSPM0 = 0100). In particular, it has been observed that faster transitions (those with shorter fall times) are more likely to be missed than slower transitions.

Work around

Insert a series resistor between the source of the $\overline{SS}$ signal and the corresponding $\overline{SS}$ input line of the microcontroller. The value of the resistor is dependent on both the application system's characteristics and process variations between microcontrollers. Experimentation and thorough testing is encouraged.

This is a recommended solution; others may exist.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: Data EEPROM

When writing to the data EEPROM, the contents of the data EEPROM memory may not be written as expected.

Work around

Either of two work arounds can be used:

1. Before beginning any writes to the data EEPROM, enable the LVD (any voltage) and wait for the internal voltage reference to become stable. LVD interrupt requests may be ignored. Once the LVD voltage reference is stable, perform all EEPROM writes normally. When writes have been completed, the LVD may be disabled.
2. Configure the BOR as enabled (any voltage). Select a threshold below V_{DD} to allow normal operation. If V_{DD} is below the BOR threshold, the device will be held in BOR Reset.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: Oscillator Configurations (OSCTUNE Register)

The INTRC and INTOSC clock sources are both adjusted using the OSCTUNE register and may not be adjusted separately. Peripherals that use the INTRC clock source (WDT and FSCM) also are affected.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: Oscillator Configurations (OSCTUNE 2 Register)

This revision of silicon does not have the OSCTUNE 2 register. Address F9Bh is not implemented.

Work around

If the INTRC frequency is to be adjusted, modify the contents of the OSCTUNE register.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: Oscillator Configurations (INTOSC Clock Source)

The INTOSC clock source requires more start-up time than what is stated in the data sheet. The IOFS bit (OSCCON<2>) will indicate the INTOSC has settled in approximately 4 ms.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (04/2003)

First revision of this document, silicon issues 1 (Data EEPROM), 2 (Internal Oscillator Block), 3 (Core), 4 (Internal Oscillator Block), 5 (INTOSC), 6 (MSSP), 7 (MSSP), 8 (INTOSC) and 9 (DC Specifications) and Data Sheet Clarification issues 1 (QFN Package), 2 (DC Characteristics Table) and 3 (Internal RC Accuracy).

Rev B Document (05/2003)

Removed silicon issue 8 (INTOSC) and modified issue 9 (DC Specifications), now issue 8. Updated Data Sheet Clarification issues 2 (DC Characteristics Table), now issue 3 and 3 (Internal RC Accuracy), now issue 2.

Rev C Document (12/2003)

Removed silicon issue 1 (Data EEPROM) and 8 (DC Specifications), added new silicon issue 7 (Data EEPROM) and removed all previous Data Sheet Clarification issues (1, 2 and 3).

Rev D Document (04/2004)

Added Data Sheet Clarification issues 1 (RE3 Pin), 2 (Timer1 Oscillator), 3 (Enhanced PWM Module Block Diagram), 4 (Enabling SPI I/O), 5 (DC Characteristics), 6 (DC Characteristics) and 7 (LVD Characteristics).

Rev E Document (02/2005)

Added Data Sheet Clarification issue 8 (PIC18F4220/4320 Pinout I/O Descriptions).

Rev F Document (03/2005)

Added Data Sheet Clarification issue 9 (Pinout I/O Descriptions).

Rev G Document (10/2007)

Removed all Data Sheet Clarifications. Added silicon issues 8-10 (Oscillator Configurations).

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