AVR515: Migrating from ATmega48/88/168 and ATmega48P/88P/168P/328P to ATtiny48/88

8-bit AVR® Microcontrollers

Application Note

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1 Introduction

This application note is a guide to assist users of ATmega48/88/168 and ATmega48P/88P/168P/328P in converting existing designs to ATtiny48/88. In addition to the differences described in this document, the electrical characteristics of the devices are different. Some of the differences are outlined in this document and some are not. Improvements or added features in ATtiny48/88 that are not in conflict with those in ATmega48/88/168 and ATmega48P/88P/168P/328P are not listed in this document.

The ATtiny48/88 are low-cost, feature-reduced versions of the ATmega48/88/168 and ATmega48P/88P/168P/328P devices. The tinyAVR versions are designed to be pin compatible with the megaAVR versions. Because of improvements that will be mentioned in this application note there may be a need for minor modifications in the application when migrating.

Please see latest data sheets for detailed information.

Rev. 8089A-AVR-09/07

2 General Porting Considerations

To make the porting process as easy as possible, one should always refer to registers and bit positions using their defined names and avoid using absolute addresses and values. In most cases, register and bit names are unchanged from device to device. When porting a design it is more convenient to include the correct definition file for the new device, rather than manually changing all addresses and bit values. It is also considered good programming practice to use named references instead of absolute values. Some examples are shown below.

```
PORTB |=  (1<<PORTB3);          // Set pin 3 on port B high
DDRB  &= ~(1<<PORTB3);          // Set pin 3 on port B as input

// Configure USI
USICR  =  (1<<USISIE)|(0<<USIOIE)|(1<<USIWM1)|(0<<USIWM0)|
          (1<<USICS1)|(0<<USICS0)|(0<<USICLK)|(0<<USITC);
```

To avoid conflicts with added features and register functionality, never access registers that are marked as reserved. Reserved bits should always be written zero, if accessed. This ensures forward compatibility, and added features will stay in their default states when unused.

3 Pin Configurations

Pin output drivers have been optimized for size in ATtiny48/88. Drive strengths are summarised in the table below.

Table 3-1. Pin drive strengths.

Supply voltage	ATmega48 ATmega88 ATmega168	ATmega48P ATmega88P ATmega168P ATmega328P	ATtiny48 ATtiny88	
			Normal I/O	High Sink
5 V	20 mA	20 mA	10 mA	20 mA
3 V	10 mA	10 mA	5 mA	10 mA

ATtiny48/88 is pin-compatible with ATmega48/88/168 and ATmega48P/88P/168P/328P by default, although some pin functions have been removed and other functions have been added. These changes should not affect pin compatibility by default but have been listed in the table below for clarity.

Table 3-2. Pin configurations.

Pin				Change
TQFP	MLF	PDIP	Name	
1	1	5	PD3	Removed: OC2B
2	2	6	PD4	Removed: XCK
3	3	-	GND (PA2)	Changed: GND to PCINT26 / PA2
6	6	-	VCC (PA3)	Changed: VCC to PCINT27 / PA3

Pin				Change
TQFP	MLF	PDIP	Name	
7	7	9	PB6	Removed: TOSC1, XTAL1. Added: CLKI
8	8	10	PB7	Removed: TOSC2, XTAL2
9	9	11	PD5	Removed: OC0B
10	10	12	PD6	Removed: OC0A
15	15	17	PB3	Removed: OC2A
19	19	-	PA0	Added: PCINT24, PA0
20	20	21	PC7	Changed: AREF to PCINT15. Added: PC7
22	22	-	PA1	Added: PCINT25, PA1
30	30	2	PD0	Removed: RXD
31	31	3	PD1	Removed: TXD

4 AVR CPU Core

The AVR core and the microcontroller architecture are the same in all AVR devices, but some instructions have not been implemented in ATtiny48/88. Where ATmega48/88/168 and ATmega48P/88P/168P/328P have 131 instructions, ATtiny48/88 only has 123. The table below summarizes instructions that are available on ATmega48/88/168 and ATmega48P/88P/168P/328P but have not been implemented in ATtiny48/88.

Table 4-1. Instructions not implemented in ATtiny48/88.

Instruction	Operands	Meaning
MUL	Rd, Rr	Multiply Unsigned
MULS	Rd, Rr	Multiply Signed
MULSU	Rd, Rr	Multiply Signed with Unsigned
FMUL	Rd, Rr	Fractional Multiply Unsigned
FMULS	Rd, Rr	Fractional Multiply Signed
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned
JMP	k	Direct Jump
CALL	k	Direct Subroutine Call

The limited instruction set is of concern chiefly when programming in assembler. High-level language (such as “C”) compilers automatically take into account the available instruction set and the end user does not need to be aware of limitations.

In applications that extensively rely on the use of multiplication and division there may be a code size and speed penalty when moving from ATmega48/88/168 and ATmega48P/88P/168P/328P to ATtiny48/88. This is because multiplication and division require more instructions and take longer time to execute in the absence of a hardware multiplier.

5 Memories

ATtiny48/88 has less volatile and non-volatile memory than ATmega48/88/168 and ATmega48P/88P/168P/328P, as shown in the table below. This means some firmware may have to be re-engineered or recompiled using memory optimisation algorithms.

Table 5-1. Memory Summary.

Device	Memory Size in Bytes		
	Flash	SRAM	EEPROM
ATmega48/48V/48P/48PV	4096	512	256
ATmega88/88V/88P/88PV	8192	1024	512
ATmega168/168V/168P/168PV	16384	1024	512
ATmega328P/328PV	32768	2048	1024
ATtiny48	4096	256	64
ATtiny88	8192	512	64

6 System Clock and Clock Options

ATtiny48/88 has a reduced clock system as compared to ATmega48/88/168 and ATmega48P/88P/168P/328P.

6.1 Clock Sources

ATtiny48/88 does not include a crystal oscillator, but all other clocking options of ATmega48/88/168 and ATmega48P/88P/168P/328P are available, as shown in the table below.

Table 6-1. Clocking Source Settings.

Device Clocking Option	CKSEL3...0	
	ATmega48/88/168 ATmega48P/88P/168P	ATtiny48/88
External Clock	0000	
Reserved	0001	
Calibrated Internal RC Oscillator	0010	
Internal 128 kHz RC Oscillator	0011	
Low Frequency Crystal Oscillator	0100	N/A[1]
	0101	
Full Swing Crystal Oscillator	0110	
	0111	
Reserved	1000 - 1111	

Notes: 1. Crystal oscillator not implemented in ATtiny48/88.

7 Power Management and Sleep Modes

ATtiny48/88 has less sleep modes than ATmega48/88/168 and ATmega48P/88P/168P/328P. The table below summarises sleep modes in all devices.

Table 7-1. Sleep Modes.

Sleep Mode	Implementation		
	ATmega48 ATmega88 ATmega168	ATmega48P ATmega88P ATmega168P ATmega328P	ATtiny48 ATtiny88
Idle	X	X	X
ADC Noise Reduction	X	X	X
Power-down	X	X	X
Power-save	X	X	
Standby	X	X	
Extended Standby		X	

Sleep mode selection bit SM2 has not been implemented in ATtiny48/88.

The BOD disable function in Extended Standby Sleep Mode of ATmega48P/88P/168P/328P can be found in the Power-down Sleep Mode of ATtiny48/88. See device data sheets for more information.

8 Interrupts

The interrupt vector table of ATtiny48/88 differs from those of ATmega48/88/168 and ATmega48P/88P/168P/328P. See table below.

Table 8-1. Interrupt vectors.

Vector Address	ATmega48/88/168	ATmega48P/88P ATmega168P/328P	ATtiny48 ATtiny88
0x000	RESET		
0x001	INT0		
0x002	INT1		
0x003	PCINT0		
0x004	PCINT1		
0x005	PCINT2		
0x006	WDT		PCINT3
0x007	TIMER2_COMPA		WDT
0x008	TIMER2_COMPB		TIMER1_CAPT
0x009	TIMER2_OVF		TIMER1_COMPA
0x00A	TIMER1_CAPT		TIMER1_COMPB
0x00B	TIMER1_COMPA		TIMER1_OVF
0x00C	TIMER1_COMPB		TIMER0_COMPA

Vector Address	ATmega48/88/168	ATmega48P/88P ATmega168P/328P	ATtiny48 ATtiny88
0x00D	TIMER1_OVF		TIMER0_COMPB
0x00E	TIMER0_COMPA		TIMER0_OVF
0x00F	TIMER0_COMPB		SPI_STC
0x010	TIMER0_OVF		ADC
0x011	SPI_STC		EE_RDY
0x012	USART_RX		ANA_COMP
0x013	USART_UDRE		TWI
0x014	USART_TX		-
0x015	ADC		-
0x016	EE_RDY		-
0x017	ANA_COMP		-
0x018	TWI		-
0x019	SPM_RDY		-

9 Timer/Counters

The Timer/Counters of ATtiny48/88 have reduced functionality as compared to those of ATmega48/88/168 and ATmega48P/88P/168P/328P.

9.1 Timer/Counter0

The 8-bit Timer/Counter0 of ATtiny48/88 does not have a PWM output stage. As a consequence, the control bits of Timer/Counter Control Register A (TCCR0A) have been changed and the Timer/Counter Control Register B (TCCR0B) has been removed. The Compare Match Output (COM0xx) and Waveform Generation Mode (WGMxx) bits of TCCR0A have been replaced by Clear Timer on Compare Match Mode (CTC0). Also, the Clock Select bits of TCCR0B have been moved to TCCR0A.

Waveform generation modes are summarised in the table below.

Table 9-1. Waveform generation modes.

ATmega48/88/168 and ATmega48P/88P/168P/328P					ATtiny48/88
WGM	**Mode**	**TOP**	**OCRx**	**TOV**	**CTC0**
000	Normal	0xFF	Immediate	MAX	0
001	Phase correct PWM	0xFF	TOP	BOTTOM	-
010	CTC	OCRA	Immediate	MAX	1
011	Fast PWM	0xFF	BOTTOM	MAX	-
100	Reserved	-	-	-	-
101	Phase correct PWM	OCRA	TOP	BOTTOM	-
110	Reserved	-	-	-	-
111	Fast PWM	OCRA	BOTTOM	TOP	-

See device datasheets for detailed explanations of Timer/Counter functions.

9.2 Timer/Counter2

The 8-bit Timer/Counter2 of ATmega48/88/168 and ATmega48P/88P/168P/328P has not been implemented in ATtiny48/88.

10 USART0

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) have not been implemented in ATtiny48/88.

11 Analogue to Digital Converter

The option to use an external voltage reference has not been implemented in ATtiny48/88. The external voltage reference pin (AREF in ATmega48/88/168 and ATmega48P/88P/168P/328P) has been replaced by a general purpose I/O pin. This means in ATtiny48/88 it is not possible to use an external bypass capacitor to stabilize the internal voltage reference.

12 Memory Programming

The differences in Fuse Bytes, Signature Bytes and the Calibration Byte are outlined in the sections below.

12.1 Fuse Bits

ATtiny48/88, ATmega48/88/168 and ATmega48P/88P/168P/328P have identical high fuse bytes, but there are some differences in the extended and low fuse bytes, as shown in the tables below.

Table 12-1. Extended Fuse Byte.

Fuse Bit	ATmega88/168 ATmega88P/168P/328P	ATmega48 ATmega48P ATtiny48/88
7…3	(not implemented)	
2	BOOTSZ1	(not implemented)
1	BOOTSZ0	(not implemented)
0	BOOTRST	SELFPRGEN

Table 12-2. Low Fuse Byte.

Fuse Bit	ATmega48/88/168 ATmega48P/88P/168P/328P	ATtiny48/88
7	CKDIV8	
6	CKOUT	
5	SUT1	
4	SUT0	
3	CKSEL3	(not implemented)
2	CKSLE2	(not implemented)
1	CKSEL1	

<table>
<tr><th>Fuse Bit</th><th>ATmega48/88/168
ATmega48P/88P/168P/328P</th><th>ATtiny48/88</th></tr>
<tr><td>0</td><td colspan="2">CKSEL0</td></tr>
</table>

12.2 Signature Bytes

Signature bytes are unique for each device, as shown in the table below.

Table 12-3. Signature bytes.

<table>
<tr><th rowspan="2">Device</th><th colspan="3">Signature Byte</th></tr>
<tr><th>0x000</th><th>0x001</th><th>0x002</th></tr>
<tr><td>ATtiny48</td><td rowspan="9">0x1E</td><td rowspan="3">0x92</td><td>0x09</td></tr>
<tr><td>ATmega48</td><td>0x05</td></tr>
<tr><td>ATmega48P</td><td>0x0A</td></tr>
<tr><td>ATtiny88</td><td rowspan="3">0x93</td><td>0x11</td></tr>
<tr><td>ATmega88</td><td>0x0A</td></tr>
<tr><td>ATmega88P</td><td>0x0F</td></tr>
<tr><td>ATmega168</td><td rowspan="2">0x94</td><td>0x06</td></tr>
<tr><td>ATmega168P</td><td>0x0B</td></tr>
<tr><td>ATmega328P</td><td>0x95</td><td>0x0F</td></tr>
</table>

12.3 Calibration Byte

In ATtiny48/88 there is only one calibration range but in ATmega48/88/168 and ATmega48P/88P/168P/328P devices there are two, as shown in the table below.

Table 12-4. Oscillator Calibration Register.

<table>
<tr><th>Device</th><th>CAL7</th><th>CAL6…0</th></tr>
<tr><td>ATmega48/88/168</td><td rowspan="2">Selects range of operation</td><td rowspan="2">Tunes frequency within the selected range</td></tr>
<tr><td>ATmega48P/88P/168P/328P</td></tr>
<tr><td>ATtiny48/88</td><td colspan="2">Tunes frequency within one, constant range</td></tr>
</table>

13 Speed Grades

The maximum frequency of ATtiny48/88 devices is lower than that of devices ATmega48/88/168 and ATmega48P/88P/168P/328P, as shown in the table below.

Table 13-1. Device speed grades.

Device	1.8 – 5.5 V	2.7 – 5.5 V	4.5 – 5.5 V
ATmega48/88/168 ATmega48P/88P/168P	N/A	10 MHz	20 MHz
ATtiny48/88	N/A	6 MHz	12 MHz
ATmega48V/88V/168V ATmega48PV/88PV/168PV	4 MHz	10 MHz	10 MHz

Device	1.8 – 5.5 V	2.7 – 5.5 V	4.5 – 5.5 V
ATmega48/88/168 ATmega48P/88P/168P	N/A	10 MHz	20 MHz
ATtiny48V/88V	4 MHz	6 MHz	6 MHz

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