ADC1003S030/040/050

Single 10 bits ADC, up to 30 MHz, 40 MHz or 50 MHz, with voltage regulator

Rev. 03 — 2 July 2012 Product data sheet

1. General description

The ADC1003S030/040/050 are a family of 10-bit high-speed low-power Analog-to-Digital Converters (ADC) for professional video and other applications. They convert the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are Transistor-Transistor Logic (TTL) and CMOS compatible, although a low-level sine wave clock input signal is allowed.

The device includes an internal voltage reference regulator. If the application requires that the reference is driven via external sources the recommendation is to use one of the ADC1004S030/040/050 family.

2. Features

- 10-bit resolution
- Sampling rate up to 50 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 4.43 MHz full-scale input at f_{clk} = 40 MHz)
- No missing codes guaranteed
- In-Range (IR) CMOS output
- Levels TTL and CMOS compatible digital inputs
- 3 V to 5 V CMOS digital outputs
- Low-level AC clock input signal allowed
- Internal reference voltage regulator
- Power dissipation only 235 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required

3. Applications

High-speed analog-to-digital conversion for:

- Video data digitizing
- Radar
- Transient signal analysis
- Global Positioning System (GPS) receiver
- ΣΔ modulators

- Cellular based stations
- Barcode scanner
- Medical imaging

4. Quick reference data

Table 1. Quick reference data

V_{CCA} = V3 to V4 = 4.75 V to 5.25 V; V_{CCD} = V11 to V12 and V28 to V27 = 4.75 V to 5.25 V; V_{CCO} = V13 to V14 = 3.0 V to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 °C to 70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V; C_L = 15 pF and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		-	30	35	mA
I_{CCD}	digital supply current		-	16	21	mA
I_{CCO}	output supply current	f_{clk} = 40 MHz; ramp input	-	1	2	mA
INL	integral non-linearity	f_{clk} = 40 MHz; ramp input	-	±0.8	±2.0	LSB
DNL	differential non-linearity	f_{clk} = 40 MHz; ramp input	-	±0.5	±0.9	LSB
$f_{clk(max)}$	maximum clock frequency	ADC1003S030TS	30	-	-	MHz
		ADC1003S040TS	40	-	-	MHz
		ADC1003S050TS	50	-	-	MHz
P_{tot}	total power dissipation	f_{clk} = 40 MHz; ramp input	-	235	305	mW

5. Ordering information

Table 2. Ordering information

Type number	Package			Sampling frequency (MHz)
	Name	Description	Version	
ADC1003S030TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	30
ADC1003S040TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	40
ADC1003S050TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	50

6. Block diagram

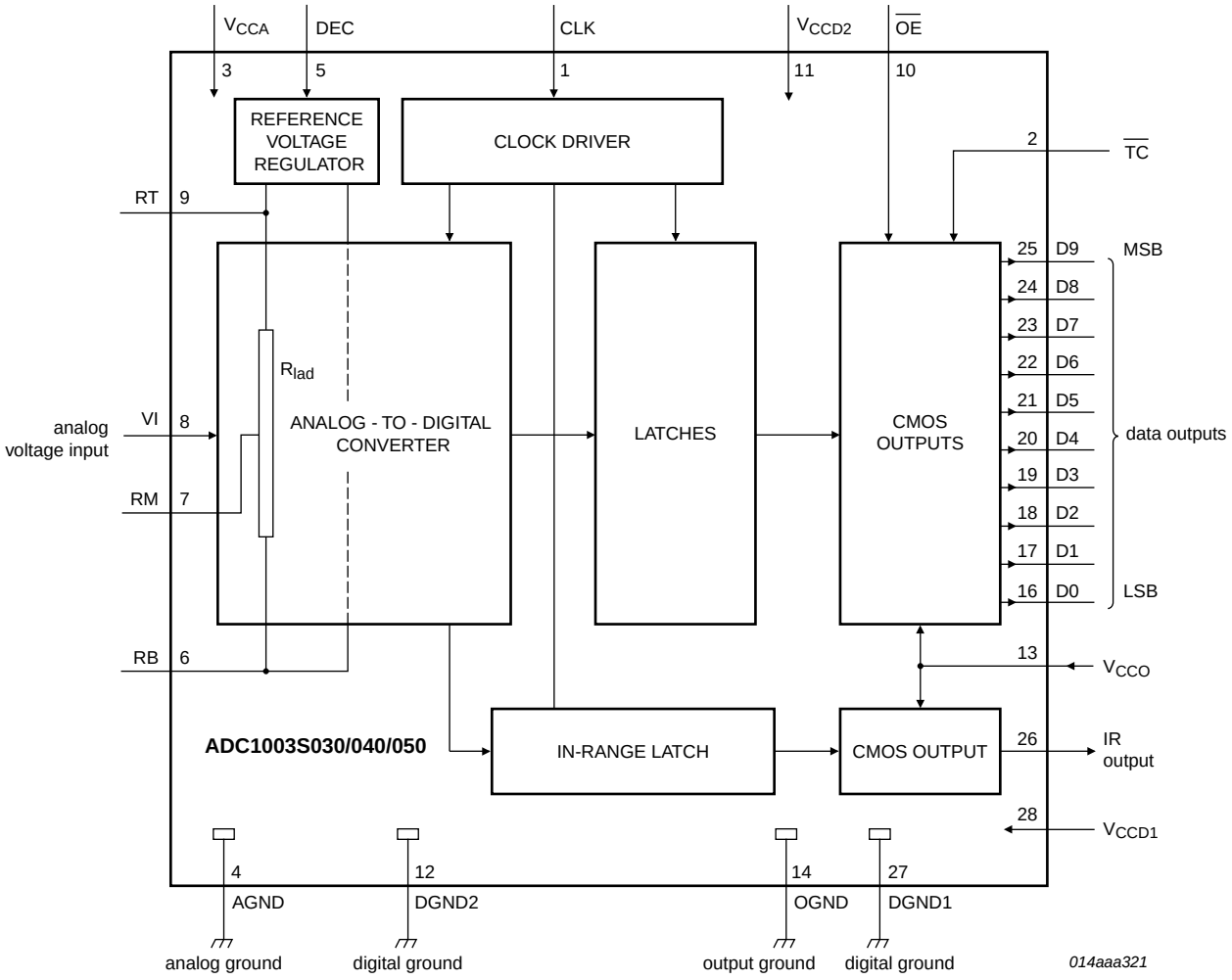


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

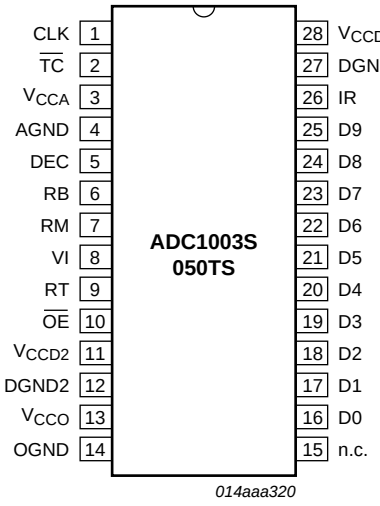


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
V_{CCA}	3	analog supply voltage (5 V)
AGND	4	analog ground
DEC	5	decoupling input
RB	6	reference voltage BOTTOM input
RM	7	reference voltage MIDDLE
VI	8	analog input voltage
RT	9	reference voltage TOP input
$\overline{OE}$	10	output enable input (CMOS level input, active LOW)
V_{CCD2}	11	digital supply voltage 2 (5 V)
DGND2	12	digital ground 2
V_{CCO}	13	supply voltage for output stages (3 V to 5 V)
OGND	14	output ground
n.c.	15	not connected
D0	16	data output; bit 0 (Least Significant Bit (LSB))
D1	17	data output; bit 1
D2	18	data output; bit 2
D3	19	data output; bit 3

Table 3. Pin description *...continued*

Symbol	Pin	Description
D4	20	data output; bit 4
D5	21	data output; bit 5
D6	22	data output; bit 6
D7	23	data output; bit 7
D8	24	data output; bit 8
D9	25	data output; bit 9 (Most Significant Bit (MSB))
IR	26	in-range data output
DGND1	27	digital ground 1
V_{CCD1}	28	digital supply voltage 1 (5 V)

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage		[1]	−0.3	+7.0	V
V_{CCD}	digital supply voltage		[1]	−0.3	+7.0	V
V_{CCO}	output supply voltage	staged	[1]	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference	$V_{CCA} - V_{CCD}$		−1.0	+1.0	V
		$V_{CCA} - V_{CCO}$		−1.0	+4.0	V
		$V_{CCD} - V_{CCO}$		−1.0	+4.0	V
V_I	input voltage	referenced to AGND		−0.3	+7.0	V
$V_{i(clk)(p-p)}$	peak-to-peak clock input voltage	referenced to DGND		-	V_{CCD}	V
I_O	output current			-	10	mA
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
T_j	junction temperature			-	150	°C

[1] The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between −0.3 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	110	K/W

10. Characteristics

Table 6. Characteristics

V_{CCA} = V3 to V4 = 4.75 V to 5.25 V; V_{CCD} = V11 to V12 and V28 to V27 = 4.75 V to 5.25 V; V_{CCO} = V13 to V14 = 3.0 V to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 °C to 70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V; C_L = 15 pF and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
ΔV_{CC}	supply voltage difference	$V_{CCA} - V_{CCD}$	−0.2	-	+0.20	V
		$V_{CCA} - V_{CCO}$	−0.2	-	+2.25	V
		$V_{CCA} - V_{CCO}$	−0.2	-	+2.25	V
I_{CCA}	analog supply current		-	30	35	mA
I_{CCD}	digital supply current		-	16	21	mA
I_{CCO}	output supply current	f_{clk} = 40 MHz; ramp input	-	1	2	mA
P_{tot}	total power dissipation	f_{clk} = 40 MHz; ramp input	-	235	305	mW
Inputs						
Clock input CLK (referenced to DGND)[1]						
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{clk} = 0.8 V	−1	0	+1	µA
I_{IH}	HIGH-level input current	V_{clk} = 2 V	-	2	10	µA
Z_i	input impedance	f_{clk} = 40 MHz	-	2	-	kΩ
C_i	input capacitance		-	2	-	pF
Inputs $\overline{OE}$ and $\overline{TC}$ (referenced to DGND)						
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	−1	-	-	µA
I_{IH}	HIGH-level input current	V_{IH} = 2 V	-	-	1	µA
VI (Analog input voltage referenced to AGND)						
I_{IL}	LOW-level input current	$V_I = V_{RB}$ = 1.3 V	-	0	-	µA
I_{IH}	HIGH-level input current	$V_I = V_{RT}$ = 3.67 V	-	35	-	µA
Z_i	input impedance	f_i = 4.43 MHz	-	8	-	kΩ
C_i	input capacitance		-	5	-	pF
Reference voltages for the resistor ladder using the internal voltage regulator see Table 7						
V_{RB}	voltage on pin RB		1.1	1.3	1.5	V
V_{RT}	voltage on pin RT		3.4	3.6	3.8	V
$V_{ref(dif)}$	differential reference voltage	$V_{RT} - V_{RB}$	2.25	2.3	2.35	V
I_{ref}	reference current		-	9.39	-	mA

Table 6. Characteristics *...continued*

V_{CCA} = V3 to V4 = 4.75 V to 5.25 V; V_{CCD} = V11 to V12 and V28 to V27 = 4.75 V to 5.25 V; V_{CCO} = V13 to V14 = 3.0 V to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 °C to 70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V; C_L = 15 pF and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{lad}	ladder resistance			-	245	-	Ω
TC_{Rlad}	ladder resistor temperature coefficient			-	456	-	mΩ/K
V_{offset}	offset voltage	BOTTOM	[2]	-	175	-	mV
		TOP	[2]	-	175	-	mV
$V_{i(a)(p-p)}$	peak-to-peak analog input voltage		[3]	1.90	1.95	2.00	V
Digital outputs D9 to D0 and IR (Referenced to OGND)							
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA		0	-	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = −1 mA		V_{CCO} − 0.5	-	V_{CCO}	V
I_{OZ}	OFF-state output current	0.5 V < V_O < V_{CCO}		−20	-	+20	μA
Switching characteristics; clock input CLK see Figure 4;[1]							
$f_{clk(max)}$	maximum clock frequency	ADC1003S030TS		30	-	-	MHz
		ADC1003S040TS		40	-	-	MHz
		ADC1003S050TS		50	-	-	MHz
$t_{w(clk)H}$	HIGH clock pulse width	full effective bandwidth		8.5	-	-	ns
$t_{w(clk)L}$	LOW clock pulse width	full effective bandwidth		5.5	-	-	ns
Analog signal processing							
Linearity							
INL	integral non-linearity	f_{clk} = 40 MHz; ramp input		-	±0.8	±2.0	LSB
DNL	differential non-linearity	f_{clk} = 40 MHz; ramp input		-	±0.5	±0.9	LSB
E_{offset}	offset error	middle code		-	±1	-	LSB
E_G	gain error	from device to device, using internal reference voltage	[4]	-	±3	-	%
Bandwidth (f_{clk} = 40 MHz)							
B	bandwidth	full-scale sine wave	[5]	-	15	-	MHz
		75 % full-scale sine wave	[5]	-	20	-	MHz
		small signal at mid-scale; V_I = ±10 LSB at code 512	[5]	-	350	-	MHz
$t_{s(LH)}$	LOW to HIGH settling time	full-scale square wave; see Figure 6	[6]	-	1.5	3.0	ns
$t_{s(HL)}$	HIGH to LOW settling time	full-scale square wave; see Figure 6	[6]	-	1.5	3.0	ns

Table 6. Characteristics *…continued*

V_{CCA} = V3 to V4 = 4.75 V to 5.25 V; V_{CCD} = V11 to V12 and V28 to V27 = 4.75 V to 5.25 V; V_{CCO} = V13 to V14 = 3.0 V to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 °C to 70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V; C_L = 15 pF and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Harmonics (f_{clk} = 40 MHz); see Figure 7 and Figure 8						
α_{1H}	first harmonic level	f_i = 4.43 MHz	-	-	0	dB
α_{2H}	second harmonic level	f_i = 4.43 MHz	-	–70	–63	dB
α_{3H}	third harmonic level	f_i = 4.43 MHz	-	–72	–63	dB
THD	total harmonic distortion	f_i = 4.43 MHz	-	–61	-	dB
Signal-to-noise ratio; see Figure 7 and Figure 8[7]						
S/N	signal-to-noise ratio	full-scale: without harmonics; f_{clk} = 40 MHz; f_i = 4.43 MHz	55	58	-	dB
Effective bits; see Figure 7 and Figure 8[7]						
ENOB	effective number of bits	ADC1003S030TS; f_{clk} = 30 MHz				
		f_i = 4.43 MHz	-	9.4		bit
		f_i = 7.5 MHz	-	9.1		bit
		ADC1003S040TS; f_{clk} = 40 MHz;				
		f_i = 4.43 MHz	-	9.3	-	bit
		f_i = 7.5 MHz	-	9.0	-	bit
		f_i = 10 MHz	-	8.9	-	bit
		f_i = 15 MHz	-	8.1	-	bit
		ADC1003S050TS; f_{clk} = 50 MHz				
		f_i = 4.43 MHz	-	9.3	-	bit
		f_i = 7.5 MHz	-	8.9	-	bit
		f_i = 10 MHz	-	8.8	-	bit
		f_i = 15 MHz	-	8.0	-	bit
Two-tone[8]						
α_{IM}	intermodulation suppression	f_{clk} = 40 MHz	-	–69	-	dB
Bit error rate						
BER	bit error rate	f_{clk} = 50 MHz; f_i = 4.43 MHz; V_I = ±16 LSB at code 512	-	10^{-13}	-	times/sample
Differential gain[9]						
G_{dif}	differential gain	f_{clk} = 40 MHz; PAL modulated ramp	-	0.8	-	%

Table 6. Characteristics *...continued*

V_{CCA} = V3 to V4 = 4.75 V to 5.25 V; V_{CCD} = V11 to V12 and V28 to V27 = 4.75 V to 5.25 V; V_{CCO} = V13 to V14 = 3.0 V to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 °C to 70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V; C_L = 15 pF and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Differential phase[9]						
φ_{dif}	differential phase	f_{clk} = 40 MHz; PAL modulated ramp	-	0.4	-	deg
Timing (f_{clk} = 40 MHz; C_L = 15 pF); see Figure 4[10]						
$t_{d(s)}$	sampling delay time		-	3	-	ns
$t_{h(o)}$	output hold time		4	-	-	ns
$t_{d(o)}$	output delay time	V_{CCO} = 4.75 V	-	10	13	ns
		V_{CCO} = 3.15 V	-	12	15	ns
C_L	load capacitance		-	-	15	pF
3-state output delay times; see Figure 5						
t_{dZH}	float to active HIGH delay time		-	5.5	8.5	ns
t_{dZL}	float to active LOW delay time		-	12	15	ns
t_{dHZ}	active HIGH to float delay time		-	19	24	ns
t_{dLZ}	active LOW to float delay time		-	12	15	ns

[1] In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 0.5 ns

[2] Analog input voltages producing code 0 up to and including code 1023:

a) V_{offset} BOTTOM is the difference between the analog input which produces data equal to 00 and the reference voltage on pin RB (V_{RB}) at T_{amb} = 25 °C.

b) V_{offset} TOP is the difference between reference voltage on pin RT (V_{RT}) and the analog input which produces data outputs equal to code 1023 at T_{amb} = 25 °C.

[3] In order to ensure the optimum linearity performance of such converter architecture the lower and upper extremities of the converter reference resistor ladder (corresponding to output codes 0 and 1023 respectively) are connected to pins RB and RT via offset resistors R_{OB} and R_{OT} as shown in Figure 3.

a) The current flowing into the resistor ladder is $I_L = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter to cover code 0 to code 1023, is $V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = 0.848 \times (V_{RT} - V_{RB})$

b) Since R_L, R_{OB} and R_{OT} have similar behavior with respect to process and temperature variation, the ratio $\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from device to device. Consequently, variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is optimized.

[4] $E_G = \frac{(V_{1023} - V_0) - V_{i(P-P)}}{V_{i(P-P)}} \times 100$

[5] The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSB, neither any significant attenuation are observed in the reconstructed signal.

[6] The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square wave signal) in order to sample the signal and obtain correct output data.

[7] Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8000 acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to signal-to-noise ratio: SINAD = ENOB × 6.02 + 1.76 dB.

[8] Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter.

[9] Measurement carried out using video analyzer VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.

[10] Output data acquisition: the output data is available after the maximum delay time of $t_{d(o)}$. For the 50 MHz version it is recommended to have the lowest possible output load.

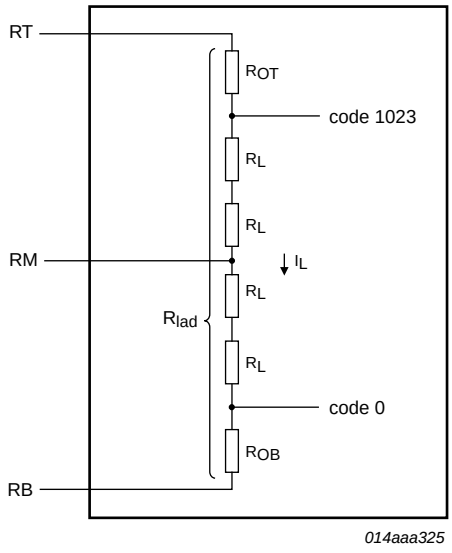


Fig 3. Explanation of Table 6 Table note 3

11. Additional information relating to Table 6

Table 7. Output coding and input voltage (typical values; referenced to AGND)

Code	$V_{i(a)(p-p)}$ (V)	IR	Binary outputs D9 to D0	Two's complement outputs D9 to D0
Underflow	< 1.455	0	00 0000 0000	10 0000 0000
0	1.455	1	00 0000 0000	10 0000 0000
1	-	1	00 0000 0001	10 0000 0001
↓	-	↓	↓	↓
511	2.43	↓	01 1111 1111	11 1111 1111
↓	-	↓	↓	↓
1022	-	11	11 1111 1110	01 1111 1110
1023	3.405	1	11 1111 1111	01 1111 1111
Overflow	> 3.405	0	11 1111 1111	01 1111 1111

Table 8. Mode selection

$\overline{TC}$	$\overline{OE}$	D9 to D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

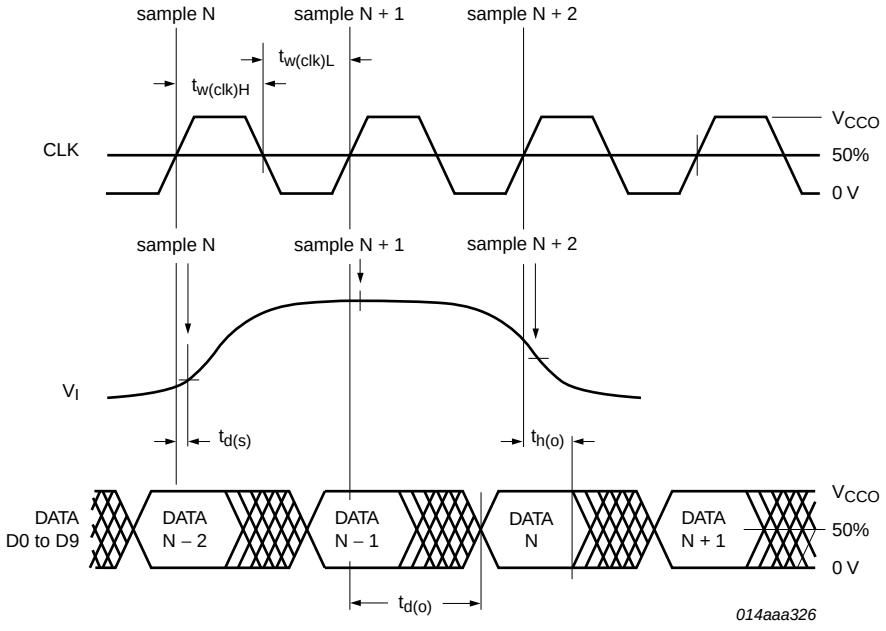
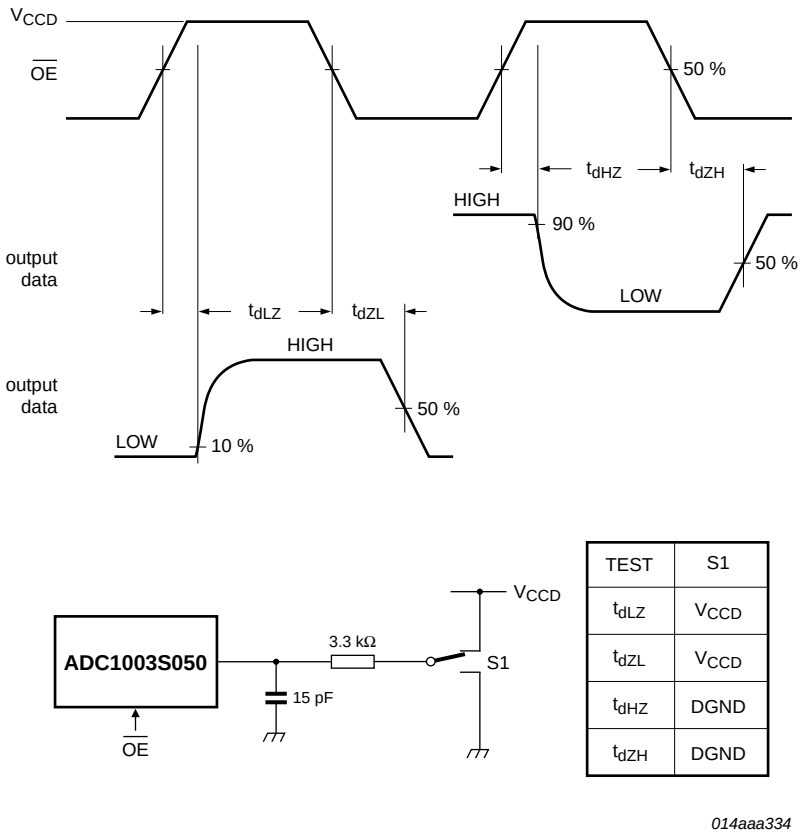


Fig 4. Timing diagram



frequency on pin $\overline{OE}$ = 100 kHz

Fig 5. Timing diagram and test conditions of 3-state output delay time.

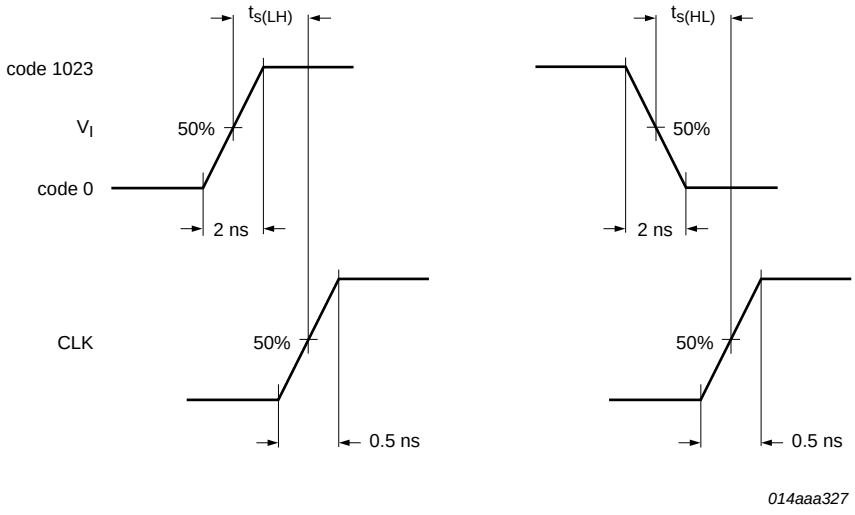
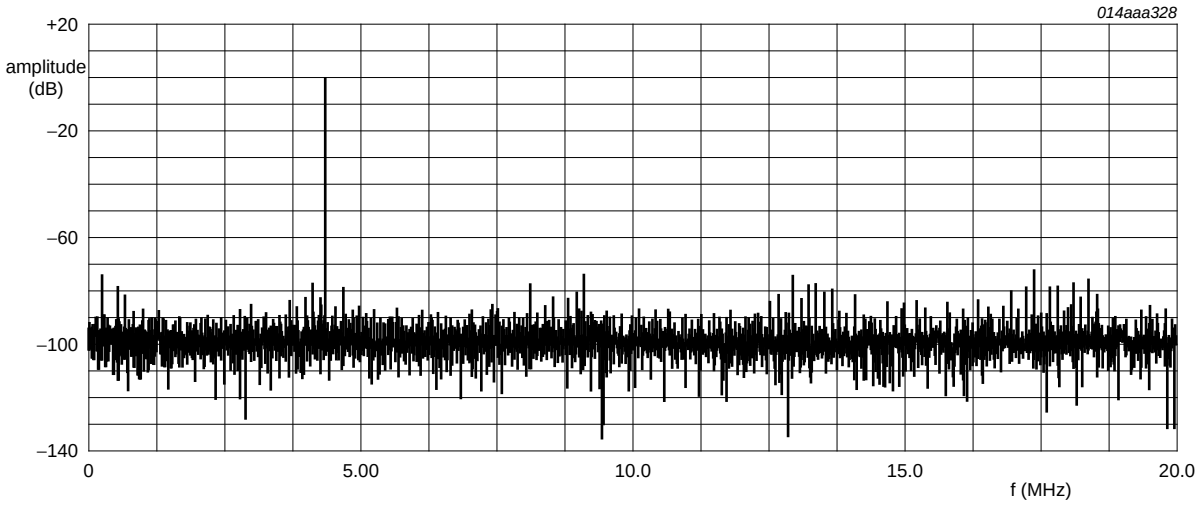


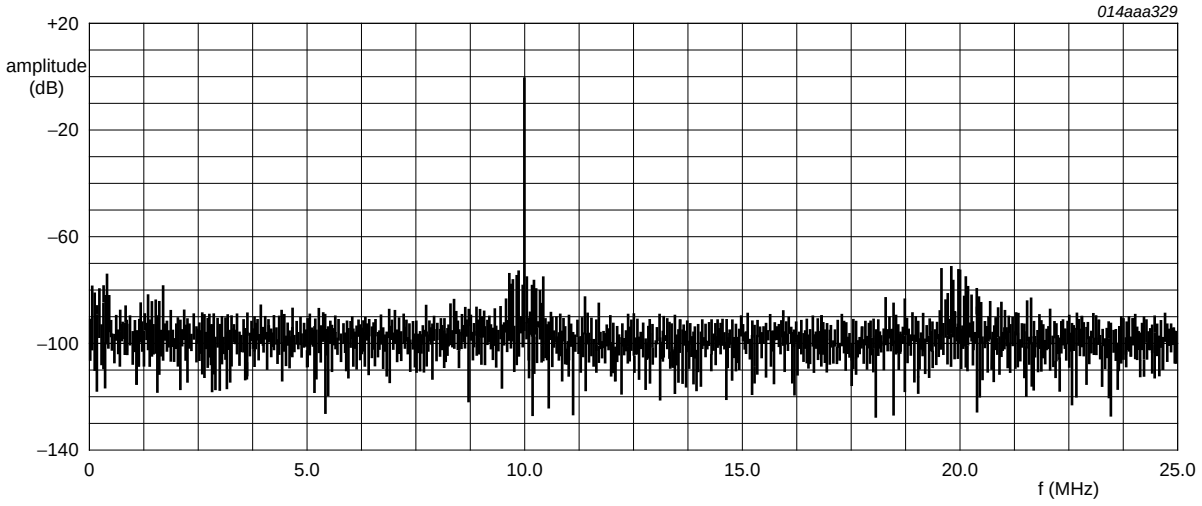
Fig 6. Analog input settling-time diagram



(1) Effective bits: 9.42; THD = −71.8 dB

(2) Harmonic levels (dB): 2nd = −83.19; 3rd = −78.09; 4th = −78.72; 5th = −78.33; 6th = −77.55

Fig 7. Typical fast Fourier transform (f_{clk} = 40 MHz; f_i = 4.43 MHz)



(1) Effective bits: 8.91; THD = −62.96 dB

(2) Harmonic levels (dB): 2nd = −71.38; 3rd = −71.54; 4th = −74.14; 5th = −65.15; 6th = −77.16

Fig 8. Typical fast Fourier transform (f_{clk} = 50 MHz; f_i = 10 MHz)

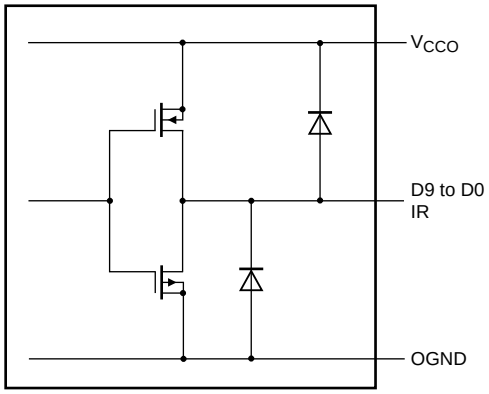


Fig 9. CMOS data and in-range outputs

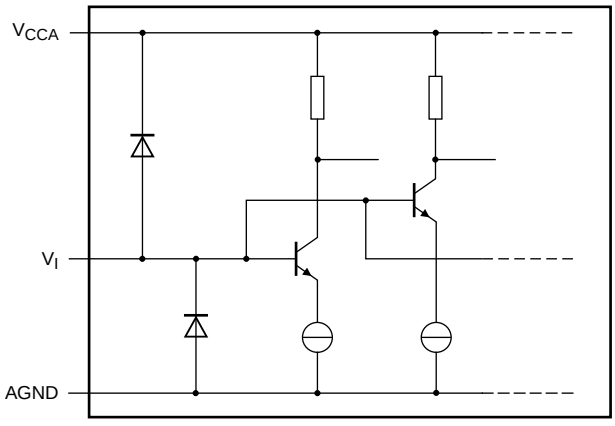


Fig 10. Analog inputs

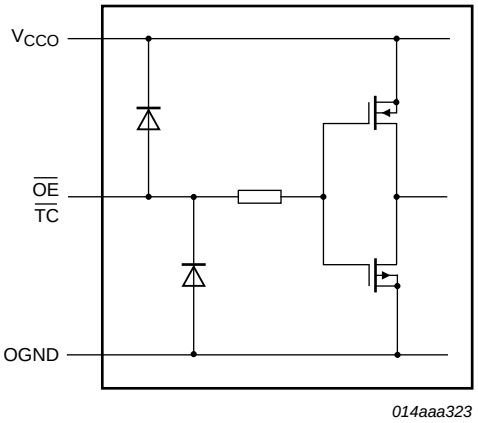


Fig 11. $\overline{OE}$ and $\overline{TC}$ input

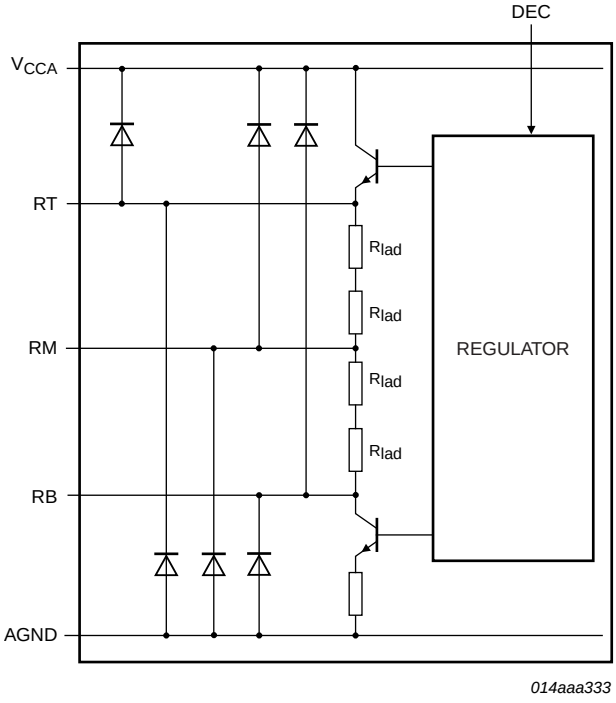


Fig 12. RB, RM and RT

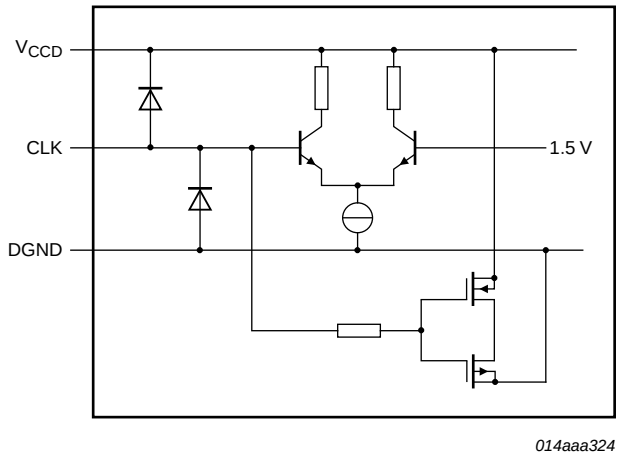
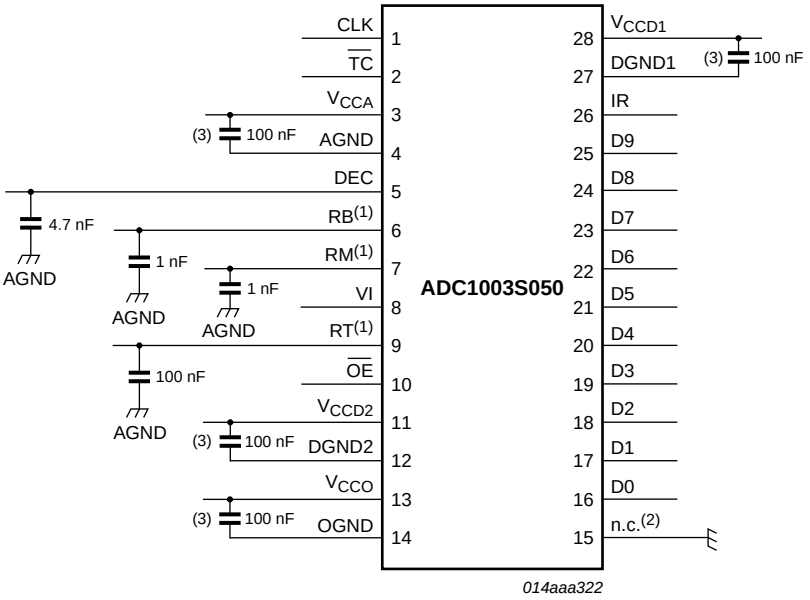


Fig 13. CLK input

12. Application information

12.1 Application diagram



The analog and digital supplies should be separated and well decoupled.

A user manual is available that describes the demonstration board that uses the ADC1003S030/040/050 family in an application environment.

(1) RB, RM and RT are decoupled to AGND.

(2) Pin 15 may be connected to DGND in order to prevent noise influence.

(3) Decoupling capacitor for supplies: must be placed close to the device.

Fig 14. Application diagram

12.2 Alternative parts

The following alternative parts are also available:

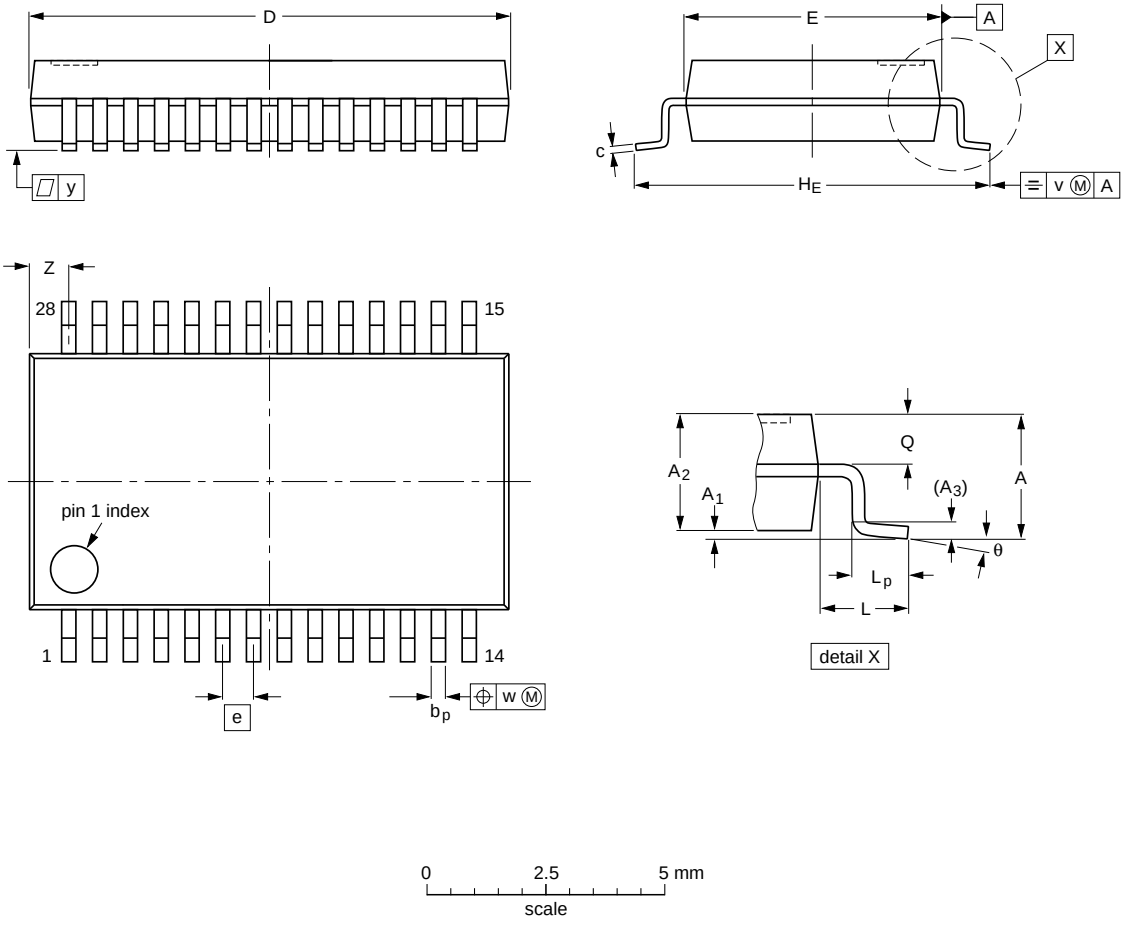
Table 9. Alternative parts

Type number	Description		Sampling frequency
ADC1004S030	Single 10 bits ADC	[1]	30 MHz
ADC1004S040	Single 10 bits ADC	[1]	40 MHz
ADC1004S050	Single 10 bits ADC	[1]	50 MHz
ADC1005S060	Single 10 bits ADC	[1]	60 MHz
ADC0804S030	Single 8 bits ADC	[1]	30 MHz
ADC0804S040	Single 8 bits ADC	[1]	40 MHz
ADC0804S050	Single 8 bits ADC	[1]	50 MHz

[1] Pin to pin compatible

13. Package outline

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT341-1		MO-150				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT341-1 (SSOP28)

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1003S030_040_050_3	20120702	Product data sheet	-	ADC1003S030_040_050_2
ADC1003S030_040_050_2	20080807	Product data sheet	-	ADC1003S030_040_050_1
Modifications:	• Corrections made to the values of ΔV_{CC} and the cross reference in subhead Reference voltages for the resistor ladder in Table 6. • Corrections made to the table notes in Figure 14.			
ADC1003S030_040_050_1	20080611	Product data sheet	-	-

15. Contact information

For more information or sales office addresses, please visit: http://www.idt.com

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