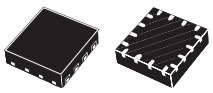
STUSB03E

USB Transceiver

General features

- Compliant to USB V2.0 for full-speed (12Mb/s) and low-speed (1.5Mbps) operation
- HBM = ±14kV on D+, D– lines; ±5kV on VBUS
- ESD Compliant to IEC-61000-4.2 (level 3) on D+, D- lines
- Separate I/O supply with operation down to 1.6V
- Integrated 3.3V output LDO
- Very low power consumption to meet USB 'suspend' current requirements
- Small QFN16 lead free package 3x3 mm^2
- No power supply sequencing requirements
- Software controlled re-enumeration
- Integrated D+ pull-up resistor for FS operation



QFN16 (3mm x 3mm)

Description

The STUSB03E is a single chip transceiver that complies with the physical layer specifications of the Universal Serial Bus (USB) v2.0 standard. It has an integrated 5V to 3.3V regulator which allows direct powering from the V_{BUS}. The transceiver has an integrated voltage detector to detect the presence of the V_{BUS} voltage and features an internal D+ pull-up resistor implemented in accordance with the 27% resistor ECN.

The STUSB03E also supports Sharing mode when V_{BUS} is not present, which allows the D+/D– lines to be shared with other serial protocols.

It supports both full-speed (12Mbps) and low-speed (1.5Mbps) operation. It is also designed to operate down to 1.6V so that it is compatible with lower system voltages of most portable systems, which include PDAs, MP3 Player and Cell phones.

Order code

Part number	Package	Packaging
STUSB03EQR	QFN16 (3mm x 3mm)	3000 parts per reel

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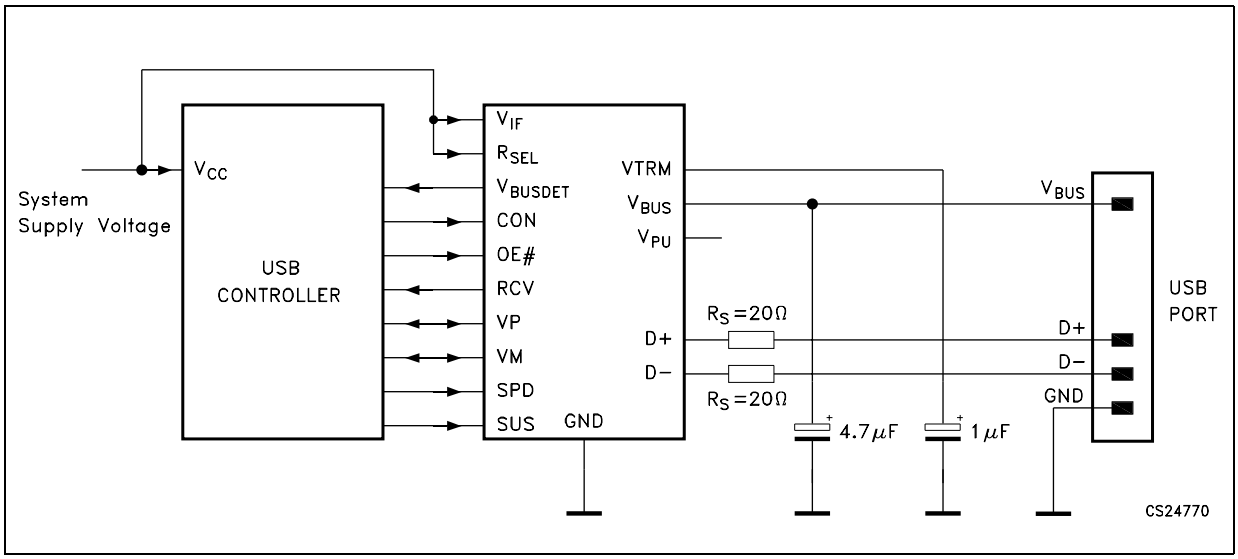
1 Typical application

Figure 1. Application circuit



2 Pin configuration

Figure 2. Pin connections (Top View)

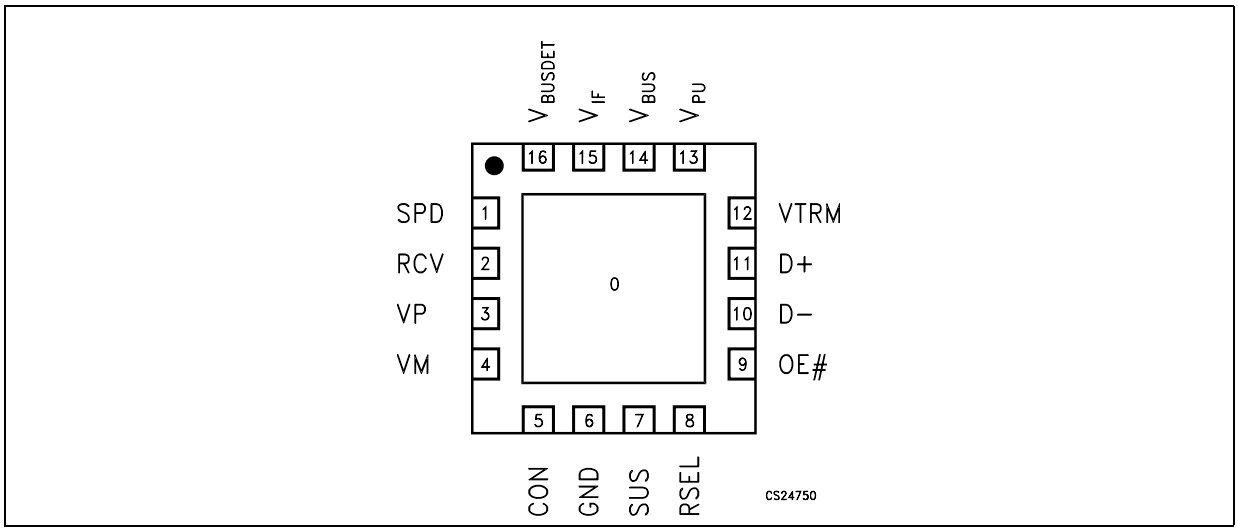


Table 1. Pin description

Pln N°	Symbol	I/O	Name and function
1	SPD	I	Speed selection input. A logic HIGH operates at edge rates for “fullspeed” operation. A logic LOW operates edge rates for “lowspeed” operation. See also CON pin.
2	RCV	O	Receive Data. Output for USB differential data. (see *Table 2*)
3	VP	I/O	If OE# = H, VP = Receiver output (+) If OE# = L, VP = Driver input (+) (see *Table 2*)
4	VM	I/O	If OE# = H, VM = Receiver output (-) If OE# = L, VM = Driver input (-) (see *Table 2*)
5	CON	I	CONNECT (input). Connects the internal pull-up resistor to D+ if SPD and RSEL are logic high. Controls status of V_{PU} pin if SPD or RSEL is logic low.
6	GND		Ground reference
7	SUS	I	Suspend (active-high). Turns off internal circuits to reduce supply current.
8	RSEL	I	Full speed pull-up resistor selection input. If RSEL = 0 the internal pull-up resistor connected to D+ is disabled and an external resistor connected to V_{PU} pin must be used.
9	OE#	I	Output Enable (active-low). Enables transceiver data transmission onto the bus. When not active, the transceiver is in the receive mode. (see *Table 2*)
10, 11	D-, D+	I/O	Differential data lines that conform to the USB v2.0 standard. (see *Table 2*)
12	VTRM	O	3.3V Reference Supply Output. Requires a 1.0µF decoupling capacitor for stability.
13	V_{PU}	O	Pull-up Supply Voltage Output. Used to connect 1.5K pull-up speed detect resistor when RSEL or SPD is logic low. If CON = 0, V_{PU} is high impedance. If CON = 1, V_{PU} = 3.3V ±10% (see *Table 4.*).
14	V_{BUS}	I	USB Bus Supply Voltage (4V to 5.5V). Supplies power to the USB transceiver and internal circuitry.
15	V_{IF}	I	System Interface Supply Voltage (1.6V to 3.6V). Provides reference supply voltage for system I/O interface signals.
16	V_{BUSDET}	O	V_{BUS} indicator output. When V_{BUS} > 4.0V, V_{BUSDET} = High; when < 3.6V, V_{BUSDET} = Low (V_{IF} referred).
EXP	N.C.		Not connected.

3 Functional tables

Table 2. Function selection

SUS	OE#	D+, D-	RCV	VP/VM	Function
L	L	Driving	Active	Active	Normal transmit mode
L	H	Receiving	Active	Active	Normal receive mode
H	L	Hi-Z	L	Not Active	Low power state
H	H	Hi-Z	L	Active	Receiving during suspend (low power state) (1)

(1) During suspend VP and VM are active in order to detect out of band signalling conditions

Table 3. Sharing mode pin configuration

Input/output	Status
V_{BUS}	Floating or connected to GND
V_{IF}	1.6V to 3.6V input
D+, D-,	High impedance
VP, VM	High
RCV	Low
SPD	High impedance
V_{BUSDET}	Low
V_{PU}	High impedance
#OE, SUS, CON	High impedance inputs

Table 4. V_{PU} Status

SPD	RSEL	CON	V_{PU}
H	H	X	High impedance
H	L	L	High impedance
H	L	H	3.3V ± 10%
L	X	L	High impedance
L	X	H	3.3V ± 10%

Table 5. Truth table during normal Mode

OE# = L					
Input		**Output**			**Result**
VP	**VM**	**D+**	**D-**	**RCV**	
L	L	L	L	X	SE0
L	H	L	H	L	Logic Low
H	L	H	L	H	Logic High
H	H	X	X	X	Undefined
OE# = H					
Input		**Output**			**RESULT**
D+	**D-**	**VP**	**VM**	**RCV**	
L	L	L	L	X	SE0
L	H	L	H	L	Logic Low
H	L	H	L	H	Logic High
H	H	X	X	X	Undefined

X = Undefined

4 Maximum ratings

Table 6. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{BUS}	Supply Voltage	6	V
V+	All other Inputs	-0.5 to 4.6	V
I_O	Output Current (D+, D-)	±50	mA
I_O	Output Current (all others)	±15	mA
I_I	Input Current	±50	mA
ESD	D+, D-, HBM (Note 3)	±14	kV
	V_{BUS} (Note 3)	±5	
	All other pins (Note 3)	±2	
T_{STG}	Storage Temperature Range	-65 to + 150	°C
T_{OPR}	Operating Temperature Range	-40 to + 85	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional Operation under these conditions is not implied.

Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

Table 7. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal Resistance Junction-Ambient	59	°C/W

5 Electrical characteristics

Table 8. DC electrical characteristics (system and USB interface) (V_{IF} = 3.6V, V_{BUS} = 5V unless otherwise noted; T_A = 25°C, specifications over temperature, -40 to 85°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BUS}	USB Supply Voltage		4		5.5	V
V_{IF}	System I/F Supply Voltage		1.6		3.6	V
V_{IL}	Low Level Input Voltage (Note 4)				$0.15V_{IF}$	V
V_{IH}	High Level Input Voltage (Note 4)		$0.85V_{IF}$			V
V_{OL}	Low Level Output Voltage (Note 4)	I_{OL} = 20µA	0		100	mV
V_{OH}	High Level Output Voltage (Note 4)	I_{OH} = -20µA	V_{IF}-100		V_{IF}	mV
I_{IL}	Input Leakage Current (Note 4)		-5		5	µA
I_{IF}	V_{IF} Supply Current (Note 7)	D+, D- are idle, SUS = 1			5	µA
		D+, D- active, C_{LOAD} = 25pF, SPD=1, f=6MHz, OE#=1 (Note 5)			2	mA
		D+, D- active, C_{LOAD} = 25pF, SPD=0, f=750kHz, OE#=1 (Note5)			220	µA
		D+, D- active, C_{LOAD} = 25pF, SPD=1, f=6MHz, OE#=0 (Note 5)			0.8	mA
		D+, D- active, C_{LOAD} = 25pF, SPD=0, f=750kHz, OE#=0 (Note 5)			120	µA
I_{BUS}	V_{BUS} Supply Current	D+, D- are idle, V_{BUS} = 5.25V Suspend Mode (SUS = 1), OE# = 1, SPD = 1			150	µA
		D+, D- are idle, V_{BUS} = 5.25V SPD = 1, SUS = 0			5	mA
		D+, D- are idle, V_{BUS} = 5.25V SPD = SUS = 0			3.5	mA
		D+, D- active, V_{BUS} = 5.25V C_{LOAD} = 50pF, SPD = 1, f = 6 MHz OE# = SUS = 0 (Note 5)			8	mA
		D+, D- active, V_{BUS} = 5.25V C_{LOAD} = 50pF, f = 6 MHz, SUS = 0 OE# = SPD = 1 (Note 5)			6	
		D+, D- active, V_{BUS} = 5.25V C_{LOAD} = 600pF, f = 750 KHz, SUS = SPD = 0 (Note 5)			3.5	
$I_{VPULEAK}$	V_{PU} Leakage Current	CON = 0, V_{PU} = 0V	-5		5	µA
$I_{VIFLEAK}$	V_{IF} Leakage Current	V_{IF} = 3.6V, V_{BUS} = 0V	-5		5	µA
V_{PU}	Pull-Up Output Voltage	I_{TERM} = 200µA, V_{BUS} = 4 to 5.25V	3		3.6	V
R_{SW}	V_{PU} Internal Switch Resistance	I_{TERM} = 10mA, V_{BUS} = 4 to 5.25V	6		11	Ω
V_{BUSDET}	V_{BUS} Comparator threshold	Supply present	4			V
		Supply lost			3.6	

Note 1. Exceeding the absolute maximum rating may damage the device.
Note 2. The device is not guaranteed to function outside its operating rating.
Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
Note 4. Specification applies to the following pins: SUS, SPD, RCV, CON, VP, VM, OE#, VBUSDET.
Note 5. Characterized specification(s), but not production tested.
Note 6. All AC parameters guaranteed by design but not production tested.
Note 7. RCV NOT LOADED

Table 9. DC electrical characteristics (system and USB interface)
(V_{IF} = 3.6V, V_{BUS} = 5V unless otherwise noted; T_A = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BUS}	USB Supply Voltage		4		5.5	V
V_{IF}	System I/F Supply Voltage		1.6		3.6	V
V_{IL}	Low Level Input Voltage (Note 4)				$0.15V_{IF}$	V
V_{IH}	High Level Input Voltage (Note 4)		$0.85V_{IF}$			V
V_{OL}	Low Level Output Voltage (Note 4)	I_{OL} = 20µA			0.1	V
V_{OH}	High Level Output Voltage (Note 4)	I_{OH} = 20µA	$0.9V_{IF}$			V
I_{IL}	Input Leakage Current (Note 4)		-5		5	µA
I_{IF}	V_{IF} Supply Current (Note 7)	D+, D- are idle, SUS = 1			5	µA
		D+, D- active, C_{LOAD} = 25pF, SPD=1, f=6MHz, OE#=1 (Note 5)		1.3		mA
		D+, D- active, C_{LOAD} = 25pF, SPD=0, f=750kHz, OE#=1 (Note5)		180		µA
		D+, D- active, C_{LOAD} = 25pF, SPD=1, f=6MHz, OE#=0 (Note 5)		0.4		mA
		D+, D- active, C_{LOAD} = 25pF, SPD=0, f=750kHz, OE#=0 (Note 5)		67		µA
I_{BUS}	V_{BUS} Supply Current	D+, D- are idle, V_{BUS} = 5.25V Suspend Mode (SUS = 1), OE# = 1, SPD = 1		88	100	µA
		D+, D- are idle, V_{BUS} = 5.25V SPD = 1, SUS = 0		4.7		mA
		D+, D- are idle, V_{BUS} = 5.25V SPD = SUS = 0		3		mA
		D+, D- active, V_{BUS} = 5.25V C_{LOAD} = 50pF, SPD = 1, f = 6 MHz OE# = SUS = 0 (Note 5)		5.5		mA
		D+, D- active, V_{BUS} = 5.25V C_{LOAD} = 50pF, f = 6 MHz, SUS = 0 OE# = SPD = 1 (Note 5)		5.2		
		D+, D- active, V_{BUS} = 5.25V C_{LOAD} = 600pF, f = 750 KHz, SUS = SPD = 0 (Note 5)		3		
$I_{VPULEAK}$	V_{PU} Leakage Current	CON = 1, V_{PU} = 0V	-5		5	µA
$I_{VIFLEAK}$	V_{IF} Leakage Current	V_{IF} = 3.6V, V_{BUS} = 0V	-5		5	µA
V_{PU}	Pull-Up Output Voltage	I_{TERM} = 200µA, V_{BUS} = 4 to 5.25V		3.3		V
R_{SW}	V_{PU} Internal Switch Resistance	I_{TERM} = 10mA, V_{BUS} = 4 to 5.25V		9		Ω
V_{BUSDET}	V_{BUS} Comparator threshold	Supply present	4			V
		Supply lost			3.6	

Note 1. Exceeding the absolute maximum rating may damage the device.
Note 2. The device is not guaranteed to function outside its operating rating.
Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
Note 4. Specification applies to the following pins: SUS, SPD, RCV, CON, VP, VM, OE#, VBUSDET.
Note 5. Characterized specification(s), but not production tested.
Note 6. All AC parameters guaranteed by design but not production tested.
Note 7. RCV NOT LOADED

Table 10. ESD performance

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ESD	IEC-1000-4-2 (D+, D-)	Air Discharge (10 pulses)		±8		KV
		Contact Discharge (10 pulses)		±6		
	IEC-1000-4-2 (V_{BUS} only)	Air Discharge (10 pulses)		±5		
		Contact Discharge (10 pulses)		±5		

Table 11. DC electrical characteristics (transceiver)
(V_{IF} = 3.6V, V_{BUS} = 5V unless otherwise noted; T_A = 25°C, specifications over temperature, -40 to 85°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LO}	Hi-Z State Data Line Leakage (Suspend Mode)	V_I = 0 to 3.3 V, SUS = 1	-10		10	µA
V_{DI}	Differential Input Sensitivity	|(D+) - (D-)|	0.2			V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold	Low to high transition	0.8	1.6	2.0	V
		High to low transition	0.8	1.1	2.0	V
V_{RHYS}	Receiver Hysteresis	V_{CM} = 0.8 V		100		mV
V_{OL}	Static Output Low	R_L = 1.5 KΩ at 3.6V (see test circuit)	0		0.3	V
V_{OH}	Static Output High	R_L = 15 KΩ at GND (see test circuit)	2.8		3.6	V
C_I	Transceiver Capacitance	Pin to GND		25		pF
Z_{DRV}	Driver Output Resistance	Steady state drive	8		24	Ω
R_{PU_D+}	D+ Data line pull-up resistance	BUS idle	900		1575	Ω
		Receive mode	1425		3090	

Table 12. DC electrical characteristics (transceiver)
(V_{IF} = 3.6V, V_{BUS} = 5V unless otherwise noted; T_A = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{LO}	Hi-Z State Data Line Leakage (Suspend Mode)	V_I = 0 to 3.3 V, SUS = 1	-2		2	µA
V_{DI}	Differential Input Sensitivity	|(D+) - (D-)|	0.2			V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold	Low to high transition	0.8	1.6	2.0	V
		High to low transition	0.8	1.1	2.0	V
V_{RHYS}	Receiver Hysteresis	V_{CM} = 0.8 V		50		mV
V_{OL}	Static Output Low	R_L = 1.5 KΩ at 3.6V (see *Test circuits*)			0.3	V
V_{OH}	Static Output High	R_L = 15 KΩ at GND (see *Test circuits*)	2.8		3.6	V
C_I	Transceiver Capacitance (3)	Pin to GND		25		pF
Z_{DRV}	Driver Output Resistance	Steady state drive		16		Ω
R_{PU_D+}	D+ Data line pull-up resistance	BUS idle		1300		Ω
		Receive mode		2200		

(3) Pins D+, D-

Table 13. AC electrical characteristics

(V_{IF} = 3.6V, V_{BUS} = 5V unless otherwise noted; T_A = 25°C.) (Note 6)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_R	Transition Rise Time (LOW SPEED)	C_L = 50pF (*Figure 5*)	75			ns
		C_L = 600pF			300	
T_F	Transition Fall Time (LOW SPEED)	C_L = 50pF (*Figure 5*)	75			ns
		C_L = 600pF			300	
T_{RFM}	Rise/Fall Time Matching (LOW SPEED)	(T_R, T_F)	80		125	%
V_{CRS}	Output Signal Crossover Voltage (LOW SPEED)		1.3		2	V
T_R	Transition Rise Time (FULL SPEED)	C_L = 50pF (*Figure 5*)	4		20	ns
T_F	Transition Fall Time (FULL SPEED)	C_L = 50pF (*Figure 5*)	4		20	ns
T_{RFM}	Rise/Fall Time Matching (FULL SPEED)	(T_R, T_F)	90		111.11	%
V_{CRS}	Output Signal Crossover Voltage (FULL SPEED)		1.3		2	V
t_{TA_OI}	Output to input turnaround time	*Figure 4.*	0		5	ns
t_{TA_IO}	Output to input turnaround time	*Figure 4.*	0		5	ns
t_{PZH}, t_{PZL}	Driver enable delay	FS, *Figure 3.*	50			ns
t_{PLZ}, t_{PHZ}	Driver disable delay	FS, *Figure 3.*	50			ns
t_{PLH} t_{PHL}	VP, VM to D+, D- Propagation Delay	FS, C_L = 50pF			55	ns
		LS, C_L =600pF			300	ns
t_{PLH} t_{PHL}	D+, D- to RCV Propagation Delay	FS, input slope = 15 ns			18	ns
t_{PLH} t_{PHL}	D+, D- to VP, VM Propagation Delay	FS, input slope = 15 ns			24	ns

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

Note 4. Specification applies to the following pins: SUS, SPD, RCV, CON, RCV, VP, VM, OE#.

Note 5. Characterized specification(s), but not production tested.

Note 6. All AC parameters guaranteed by design but not production tested.

6 Timing diagram

Figure 3. Driver enable and disable delay

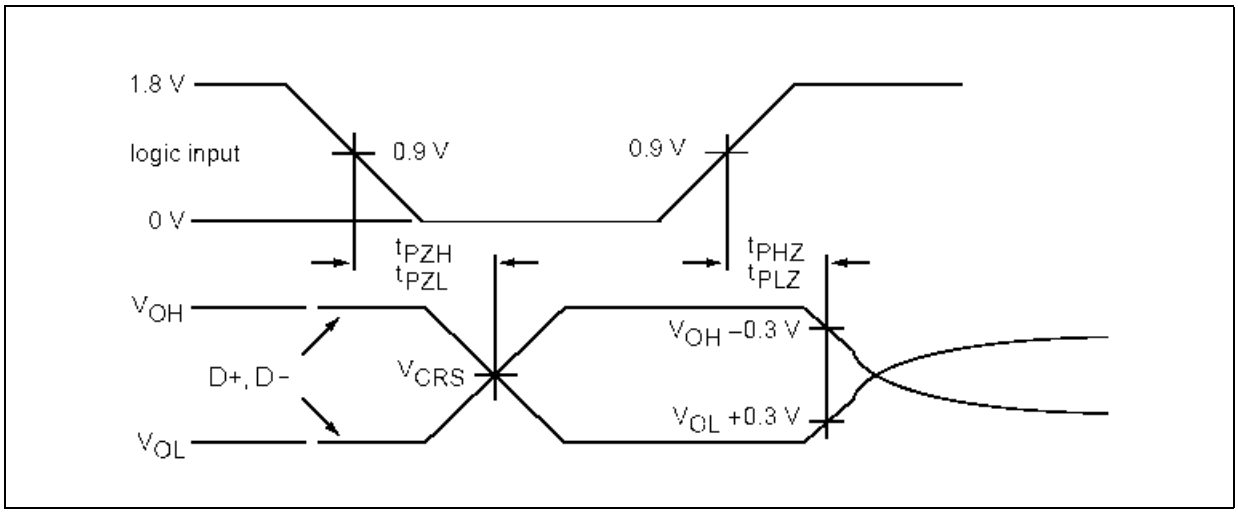


Figure 4. Turnaround time

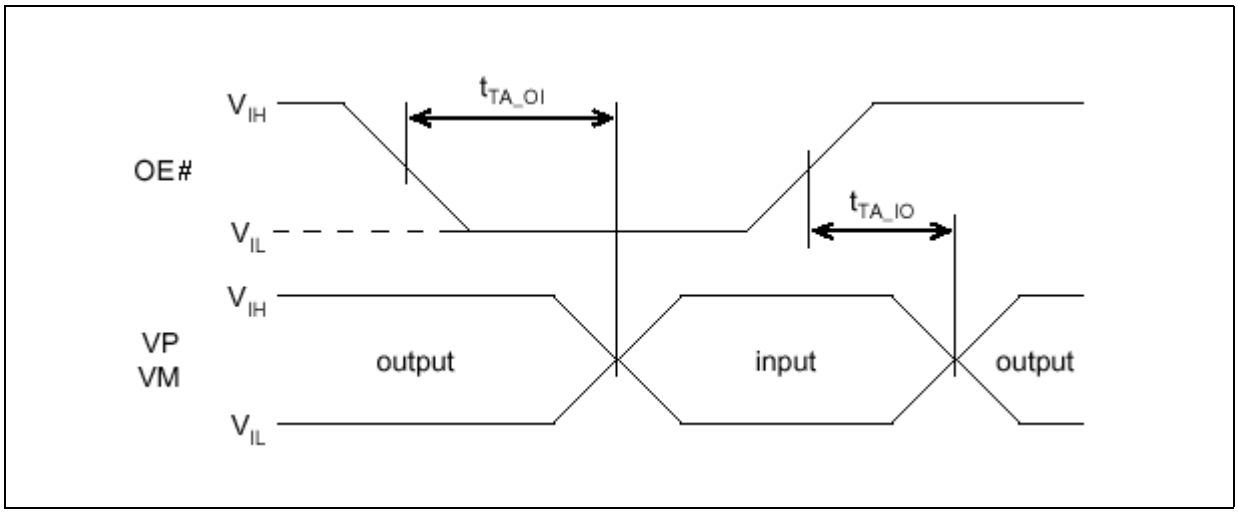


Figure 5. Rise and fall times

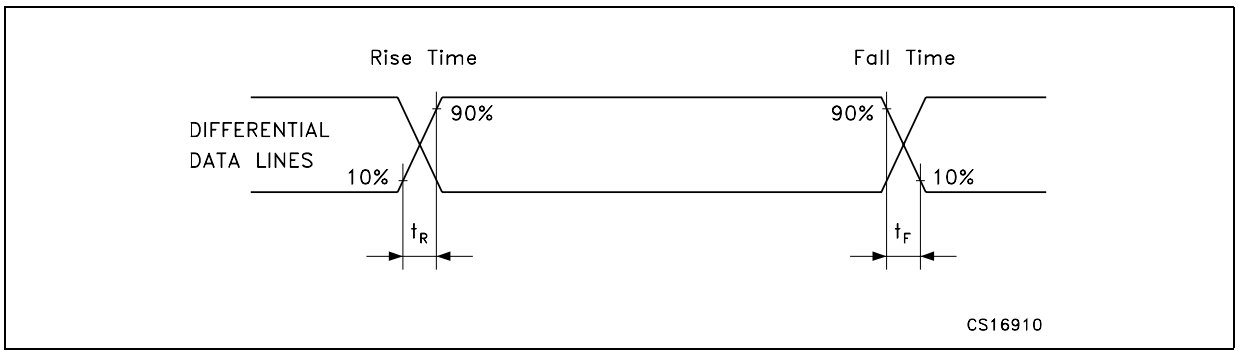


Figure 6. Receiver propagation delay

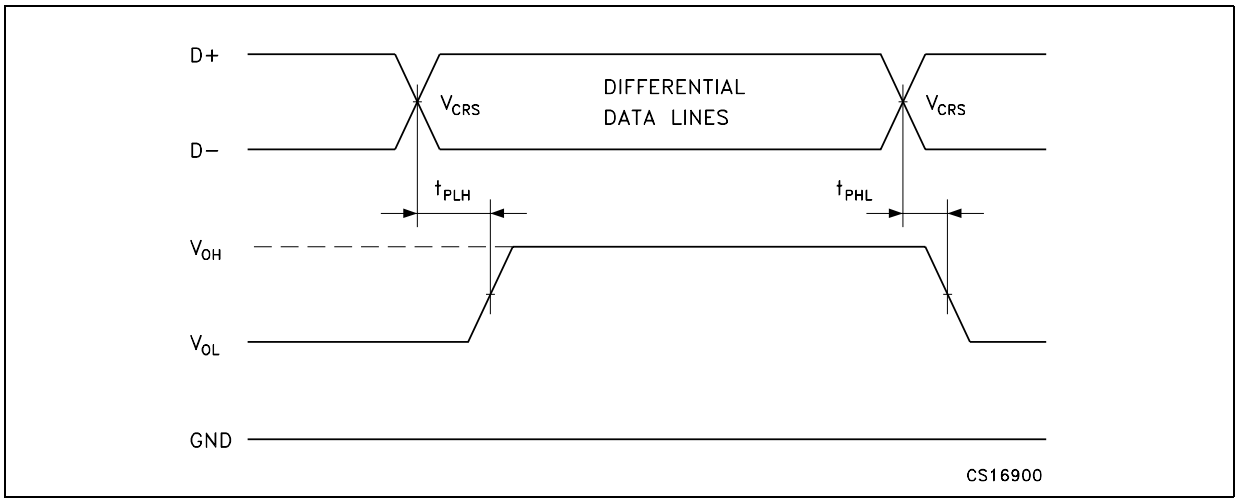
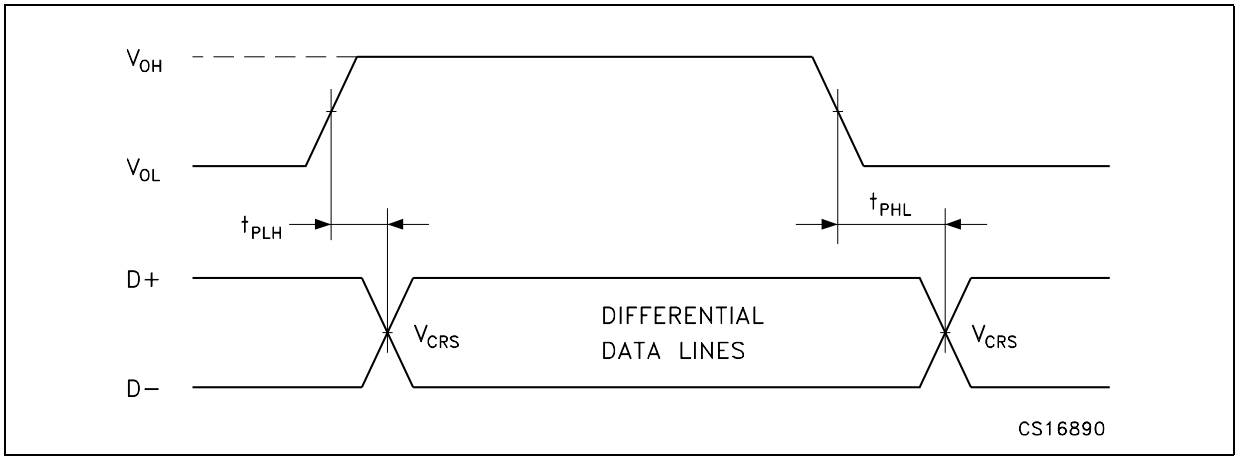
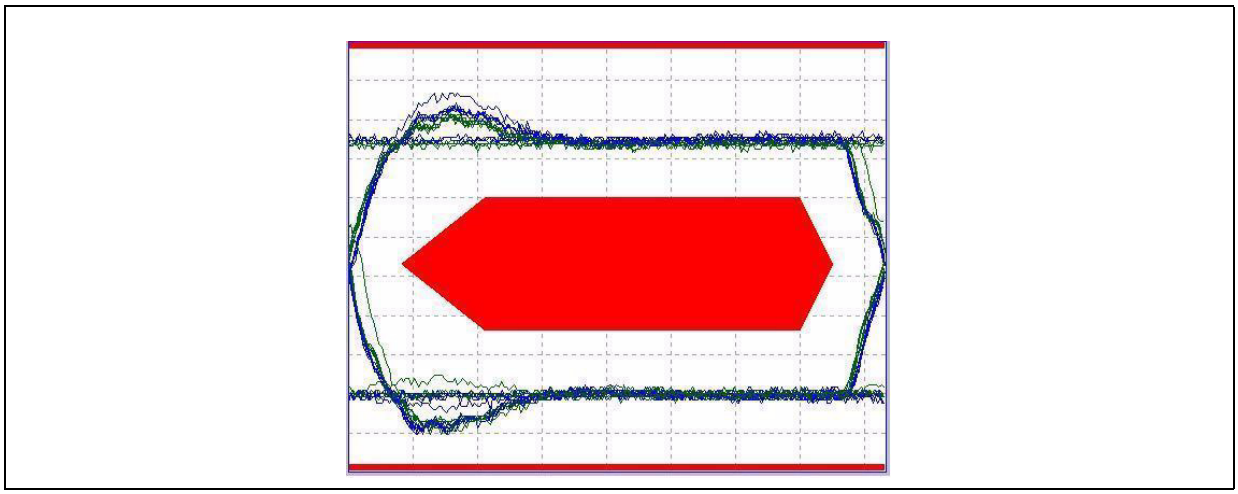


Figure 7. Driver propagation delay (C_L = 50pF)



Minimum Timing LS and maximum timing FS

Figure 8. FS eye diagram



7 Test circuits

Figure 9. Load for VP, VM, RCV

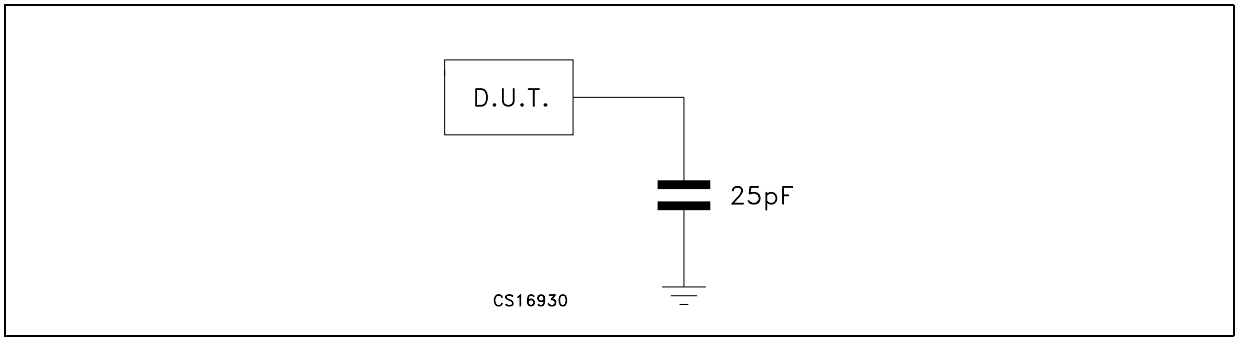


Figure 10. Load for D+, D-

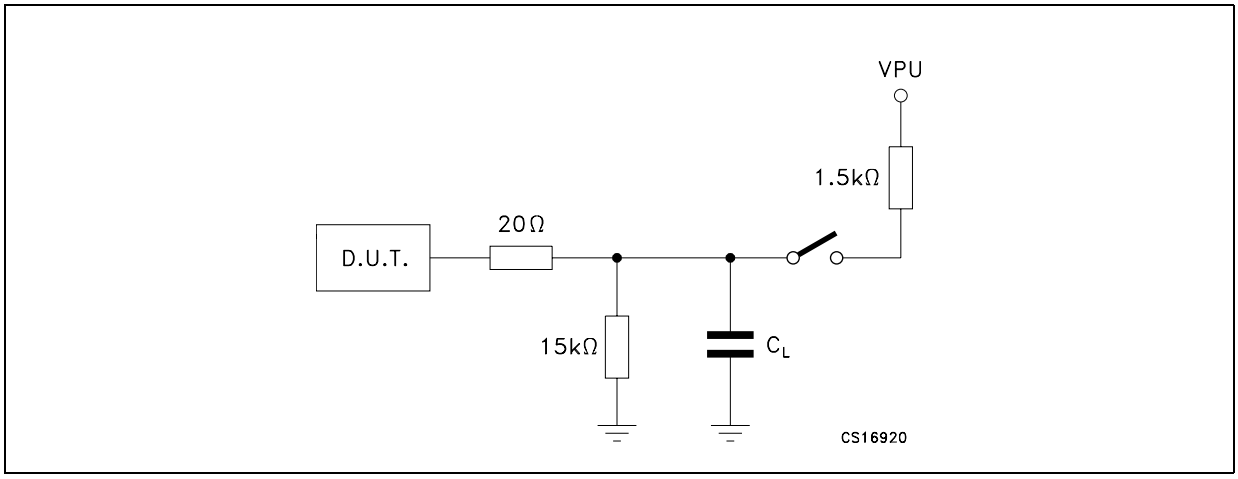
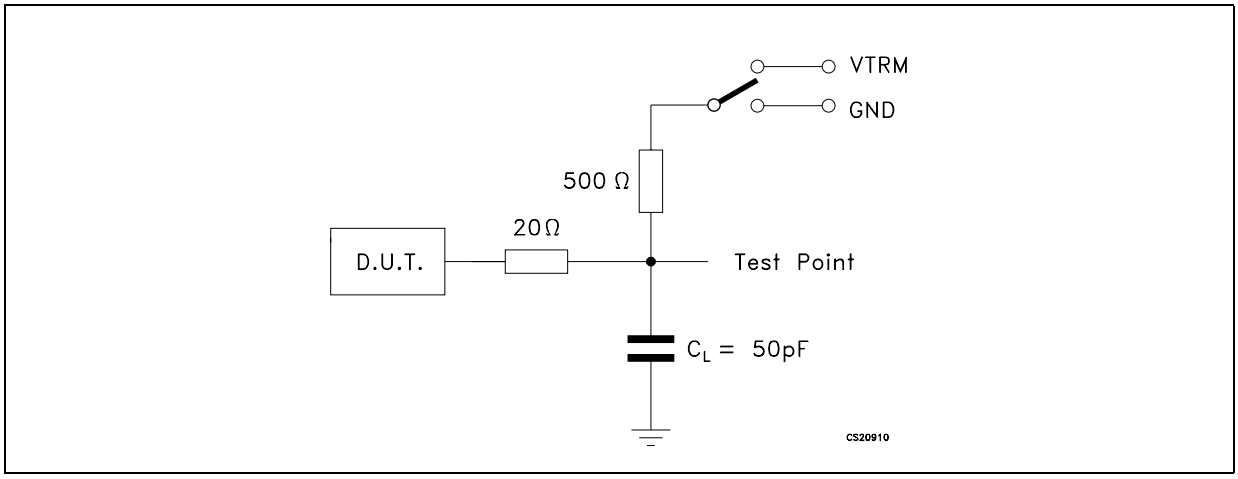
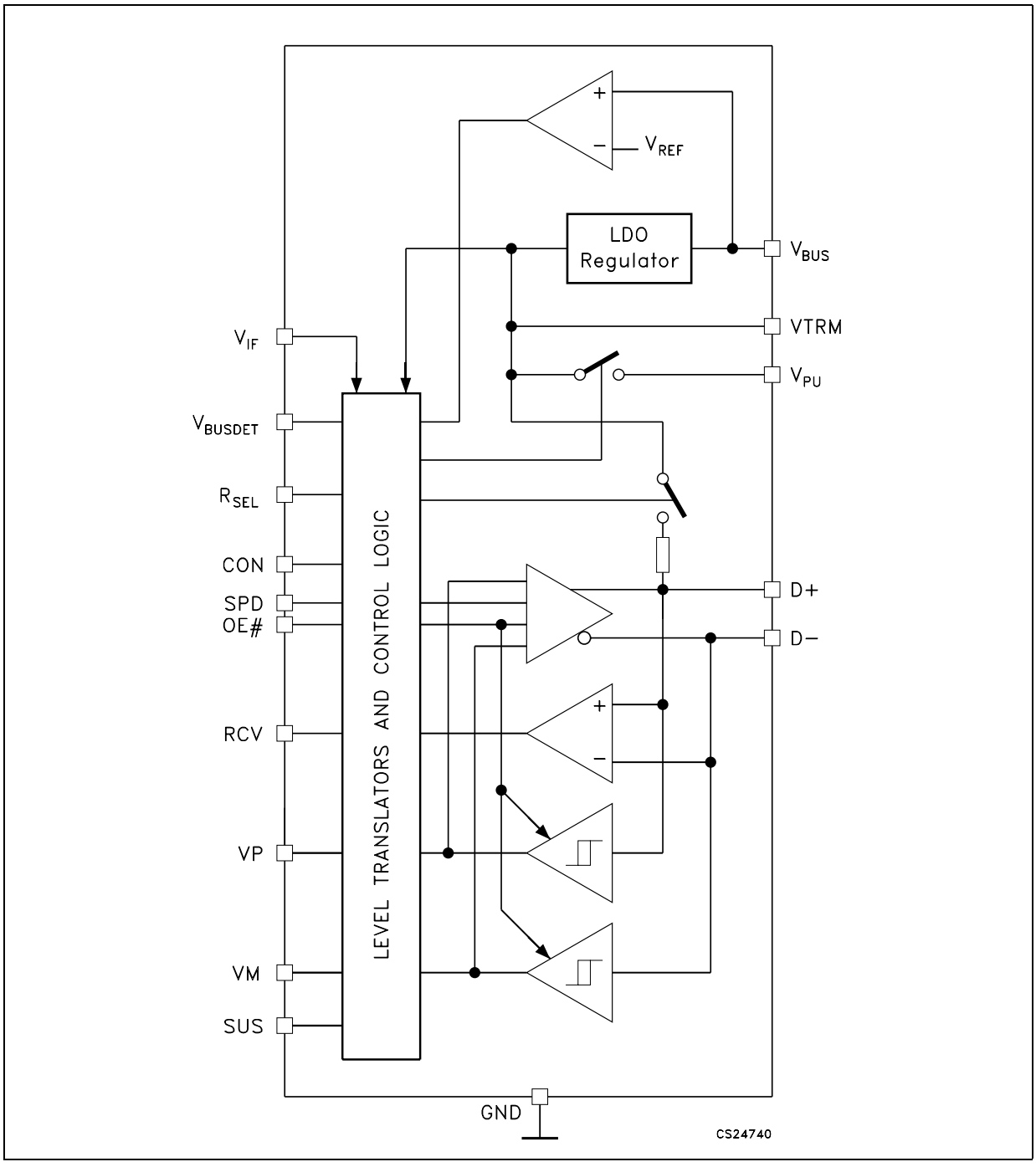


Figure 11. Enable and disable time circuit



Switch = GND for t_{PZH} and t_{PHZ}; V = VTRM for t_{PZL} and t_{PLZ}

Figure 12. Functional diagram



8 Functional description

The STUSB03E is designed to provide USB connectivity in mobile systems where available system supply voltages are not able to satisfy USB requirements. The STUSB03E can operate down to supply voltages of 1.6V and still meet USB physical layer specifications. As shown in the circuit above, the STUSB03E takes advantage of the USB supply voltage, V_{BUS}, to operate the transceiver. The system voltage, V_{IF}, is used to set the reference voltage used by the digital I/O lines interfacing to the system controller. Internal circuitry provides translation between the USB and system voltage domains. V_{IF} will typically be the main supply voltage rail for the controller.

In addition, a 3.3V, 10% termination supply voltage, V_{PU}, is provided to support speed selection. V_{PU} can be disabled or enabled under software control via the CON input. This allows for software-controlled connect or disconnect states. A 1.5K resistor is required to be connected between this pin and the D- line when operating in low speed mode. In full speed mode either an internal pull-up resistor or an external one connected between V_{PU} pin and D+ line can be used; the desired configuration is chosen by tying R_{SEL} pin to V_{IF} or GND.

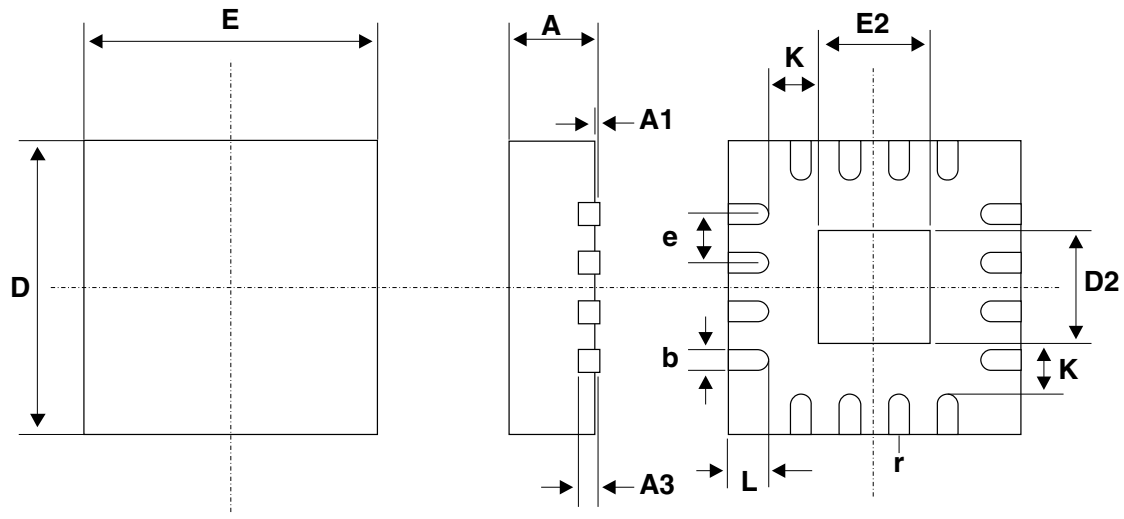
The use of ESD transient protection devices is not required for operation, but is recommended.

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

QFN16 (3mmx3mm) MECHANICAL DATA

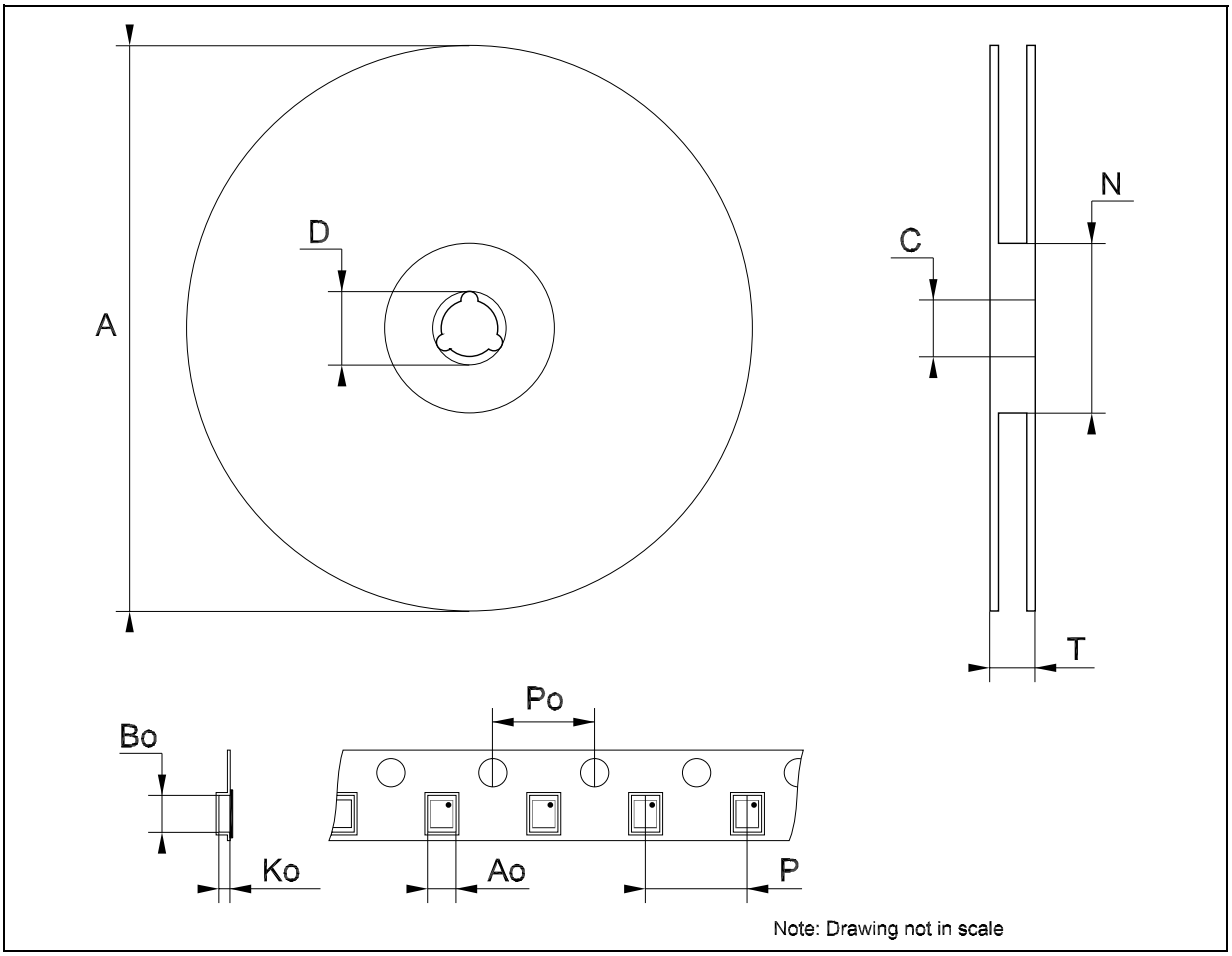
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		3.00			0.118	
D2	1.55	1.70	1.80	0.061	0.067	0.071
E		3.00			0.118	
E2	1.55	1.70	1.80	0.061	0.067	0.071
e		0.50			0.020	
K		0.20			0.008	
L	0.30	0.40	0.50	0.012	0.016	0.020
r	0.09			0.006		



This drawing is not to scale

Tape & Reel QFNxx/DFNxx (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

10 Revision history

Table 14. Revision history

Date	Revision	Changes
31-Oct-2006	1	First Release.
14-Mar-2007	2	Update tape & reel.

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