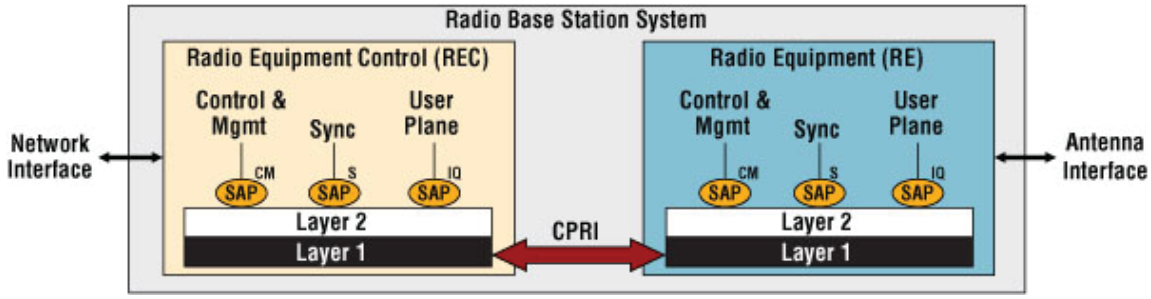
Common Public Radio Interface - CPRI IP Core

Overview

The Lattice **Common Public Radio Interface (CPRI)** IP core together with SERDES and Physical Coding Sublayer (PCS) functionality integrated in the **LatticeECP3**, **LatticeECP2M**, **LatticeSC/M** FPGAs implements the physical layer of the CPRI specification and interleaves IQ data with synchronization, control and management information. It can be used to **connect Radio Equipment Control (REC) and Radio Equipment (RE) modules**.



Features

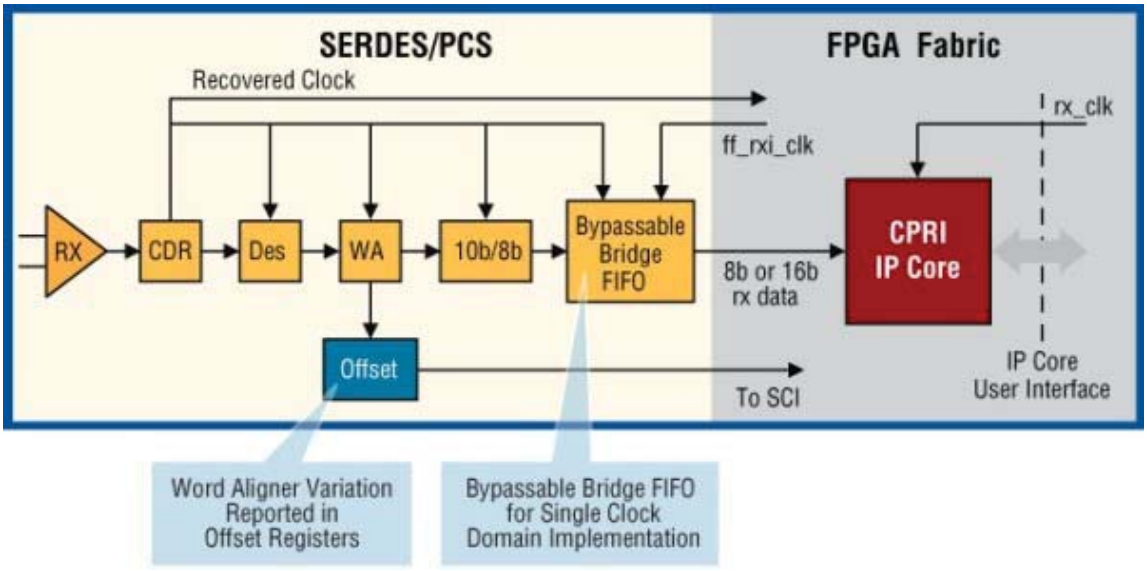
- Supports the physical link layer (Layer 1) of the CPRI specification
- Supports three standard bit rates of the CPRI specification
  - 614.4 Mbps
  - 1228.8 Mbps
  - 2457.6 Mbps
  - 3072 Mbps
- Supports 8b/10b encoding/decoding performed in the PCS/SERDES
- Supports code-violation detection performed in the PCS/SERDES
- Performs CPRI Hyperframe Framing
  - Performs interleaving of IQ data, sync, C&M data, and vendor specific information
  - Provides an 8-, 16-, or 32-bit parallel interface for IQ data
- Performs subchannel mapping:
  - Supports a slow C&M channel based on a serial HDLC interface at standard bit rates (240 Kbps, 480 Kbps,960 Kbps, and 1920 Kbps). The HDLC framer, if needed, must be provided as a separate IP core.
  - Supports a fast C&M channel based on a serial Ethernet interface (84.48 Mbps max.) to the user logic, anon-standard rate MII Ethernet interface to a MAC, or a 100 Mbps MII interface to a PHY device. Accepts a user-selected pointer to the CPRI subchannel where the Ethernet link starts. The
- Performs synchronization and timing as defined in section 4.2.8 of the CPRI Specification
- Supports the L1 Inband Protocol
- Provides a parallel interface for merging vendor specific data into the CPRI frame
- Provides a start-up sequence state machine in hardware for both REC and RE nodes which performs:
  - Synchronization and Rate Negotiation
  - C&M Plane setup
- Performs Link Maintenance as defined in section 4.2.10 of the CPRI Specification:
  - LOS detection
  - LOF detection
  - RAI indication
- Optional top-level template that implements user registers for control and status management
- Optional 8-bit register interface through the JTAG port

Ethernet MAC function isprovided as a separate IP core.

Low Latency option for LatticeECP2M/S, LatticeECP3

The low latency CPRI core configuration supports all of the features specified for the basic core configuration with the following key exceptions/modifications:

- Supports the LatticeECP2M/S and LatticeECP3 FPGAs only
- Supports 1228.8 Mbps, 2457.6 Mbps and 3072.0 Mbps line bit rates only
- FPGA bridge FIFOs in the SERDES/PCS block are bypassed in both the receive and transmit directions
- Logic blocks supporting receive direction 10b word alignment, 10b/8b decoding and core-violation detection in the SERDES/PCS block are bypassed and the corresponding functions are implemented in FPGA gates



Resource Utilization

LatticeECP3[1]

Configuration		SLICEs	LUTs	Registers	sysMEM EBRs
Serial	Low Latency	1139	1359	1522	4
Matched	Low Latency	1342	1714	1632	2
Fixed	Low Latency	1433	1848	1691	6

1. Performance and utilization data are generated targeting an LFE3-95E-7FN1156CES device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

LatticeECP2M/S[1]

Configuration		SLICEs	LUTs	Registers	sysMEM EBRs
Serial	Basic	973	1268	1120	2
Matched	Basic	1192	1654	1264	2
Fixed	Basic	1258	1796	1318	6
Serial	Low Latency	1522	2040	1429	2

Configuration		SLICEs	LUTs	Registers	sysMEM EBRs
Matched	Low Latency	1743	2432	1576	2
Fixed	Low Latency	1809	2574	1630	6

1. Performance and utilization data are generated targeting an LFE2M35E-5F672C device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M/S family.

LatticeSC/M[1]

Configuration		SLICEs	LUTs	Registers	sysMEM EBRs
Serial	Basic	913	1270	1123	2
Matched	Basic	1267	1646	1267	2
Fixed	Basic	1321	1769	1321	6

1. Performance and utilization data are generated targeting an LFSC3GA25E-5F900C or LFSCM3GA25EP1-5F900CES device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSC/M family.

Demos

LatticeECP3 CPRI Demo

Watch the LatticeECP3 CPRI Video

Ordering Information

Family	Part Number
LatticeECP3	CPRI-E3-U4
LatticeECP2M/S	CPRI-PM-U4
LatticeSC/M	CPRI-SC-U4

IP Version: 3.3

Evaluate: To download a full evaluation version of this IP, go to the IPexpress tool and click the IP Server button in the toolbar. All LatticeCORE IP cores and modules available for download will be visible. For more information on viewing/downloading IP please read the **IP Express Quick Start Guide**.
Purchase: To find out how to purchase the IP Core, please contact your **local Lattice Sales Office**.