AN2621
Application note

TS488/9 low power stereo headphone amplifier evaluation board user guidelines

Introduction

This application note concerns the evaluation board DEMOTS488/9, designed to evaluate the TS488 or TS489 pop-free 120mW stereo headphone amplifier.

In this document, you will find:

- a brief description of the TS488/9 low power stereo audio amplifier
- a description of the evaluation board and all of its components
- the layout of the evaluation board

About the TS488, TS489

The TS488/9 is an enhancement of TS486/487 that eliminates pop & click noise. It is a dual audio power amplifier capable of driving, in single-ended mode, either a 16Ω or a 32Ω stereo headset.

It delivers up to 31mW per channel (into 16Ω loads) of continuous average power with 0.1% THD+N in the audio bandwidth from a 2.5V power supply.

An externally-controlled standby mode reduces the supply current to 10nA (typical). The TS488/9 is unity gain stable and is configured by external gain-setting resistors.

Key features of the TS488/9 include:

- Pop & click noise protection circuitry
- Operating range from V_{CC} = 2.2V to 5.5V
- Standby mode active low (TS488) or high (TS489)
- Output power:
  - 120mW @5V, into 16Ω with 0.1% THD+N max (1kHz)
  - 55mW @3.3V, into 16Ω with 0.1% THD+N max (1kHz)
- Low current consumption: 2.7mA max @5V
- Ultra low standby current consumption: 10nA typical
- High signal-to-noise ratio
- High crosstalk immunity: 102dB (F = 1kHz)
- PSRR: 70dB typ. (F = 1kHz), inputs grounded @5V
- Unity-gain stable
- Short-circuit protection circuitry
- Available in lead-free MiniSO-8 and DFN8 2mm x 2mm

For complete information about the TS488/9, refer to the datasheet.

1 Description of the evaluation board

The DEMOTS488/9 is an evaluation board designed for the TS488/9 pop-free 120mW stereo headphone amplifier.

The gain (A_V) is set at 1 V/V for both channels and can be adapted if necessary with a modification of R11 or R12 values for channel 1, and of R21 or R22 values for channel 2.

Table 1. Gain per channel

Channel	Gain (V/V)
Channel 1	$A_V = -\frac{R12}{R11}$
Channel 2	$A_V = -\frac{R22}{R21}$

C11 with R11 (or C21 with R21) create an input high-pass filter with a cut-off frequency of 24.1Hz.

C13 with a 16Ω load (or C23 with a 32Ω load) create an output high-pass filter with a cut-off frequency of 45.2Hz (22.6Hz). For information on how to change the value of the cut-off frequency, refer to the datasheet.

The C12 and C22 component locations are left empty in order to add a low-pass filter if required.

Table 2. Evaluation board connectors

Connector	Description
P1	Power connector (V_{CC} and GND). Power supply voltage from 2.2V to 5.5V
P2	Standby control connector: –  pins 1 and 2 are shorted, TS488 operation mode, TS489 standby mode –  pins 2 and 3 are shorted, TS488 standby mode, TS489 operation mode The connector pins are as follows: – 1: V_{CC} – 2: Standby control – 3: GND
P10	Input signal connector (GND and active input signal). The pin 1 and 2 for the input 1 and the pin 3 and 4 for the input 2
P20	Output signal connector (GND and active output signal). The pin 1 and 2 for the output 1 and the pin 3 and 4 for the output 2

Caution: When you apply the power supply through P1, **do not** invert the polarity because it would destroy the amplifier at U1.

Figure 1. Schematic diagram

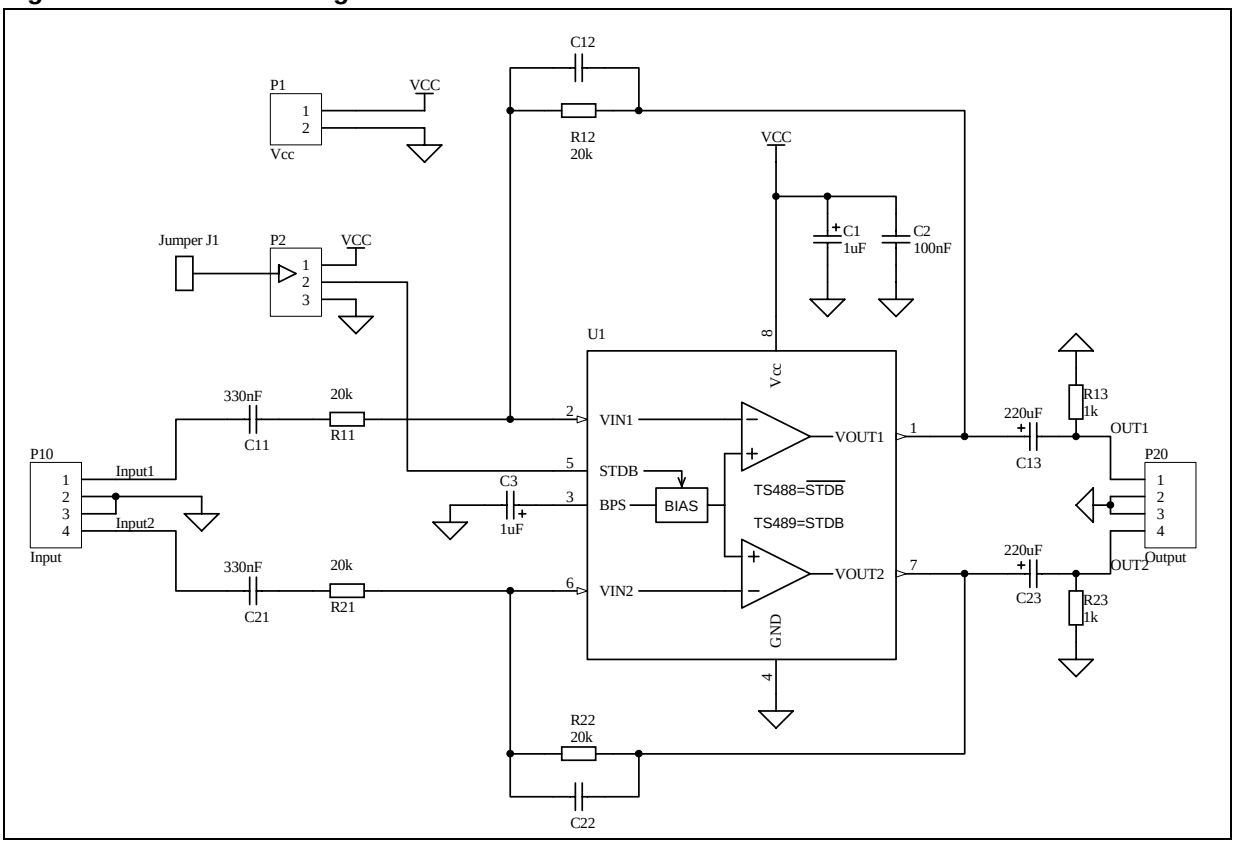


Table 3. Component list for the evaluation board

Designation	Quantity	Description
C11, C21	2	330nF/16V, ceramic capacitors, 0805
C12, C22	0	Not assembled, 0603
C2	1	100nF/16V, ceramic capacitors, 0805
C1, C3	2	1µF/50V, electrolytic capacitor, 1206
C13, C23	2	220µF/10V, electrolytic capacitor
P1	1	2-pin header 2.54mm pitch
P2	1	3-pin header 2.54mm pitch
P10, P20	2	4-pin header 2.54mm pitch
J1	1	Jumper, 2.54mm pitch
U1	1	TS488 or TS489

2 Evaluation board layout

The following schematics show the layers and the top view of the evaluation board.

Figure 2. PCB top layer

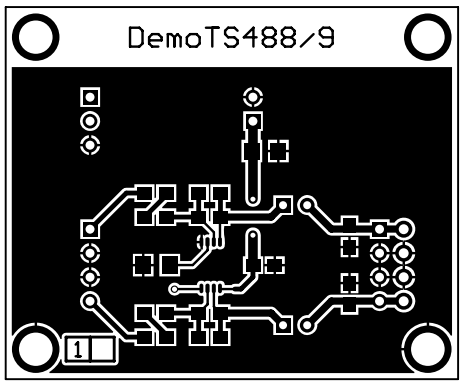


Figure 3. PCB bottom layer

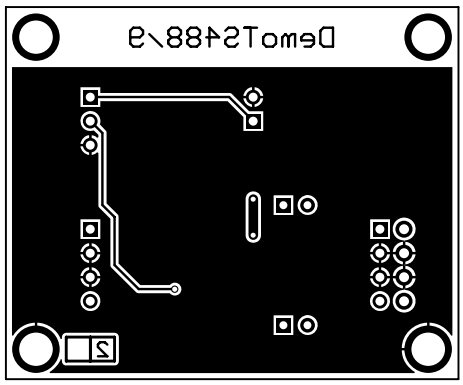
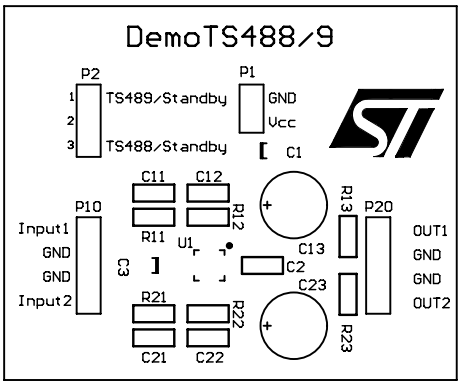


Figure 4. Top view of evaluation board



3 Revision history

Table 4. Document revision history

Date	Revision	Changes
25-Sep-2007	1	Initial release.

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