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eZ80Acclaim!® Microcontrollers

eZ80F91 Modular Development Kit

User Manual

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Revision History

Each instance in the table below reflects a change to this document from its previous edition. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page
Jan 2012	10	Modified references to eZ80F91 Modular Development Kit and supporting documentation; added PHY section; updated physical dimensions, Figures 12 and 13.	1, 23, 24, 34, 35
Jul 2008	09	Updated Figures 12 and 13.	34, 35
May 2008	08	Updated Table 1, I/O Mini-Module Connector J2 section; updated Table 2, Peripheral Bus External Connector JP1 section; added Figures 12 and 13; updated for style.	6, 9, 9, 12, 34, 35, All

Table of Contents

Introduction

Zilog's eZ80F91 Modular Development Kit, represented by part numbers eZ80F910100KITG and eZ80F910200KITG, provides a general-purpose platform for creating a design based on an eZ80F91 microcontroller. The eZ80F91 MCU is a member of Zilog's eZ80Acclaim! product family, which offers an on-chip Flash capability. The eZ80F91 Modular Development Kit contains an eZ80F91 Module (which features the eZ80F91 MCU) plus an eZ80Acclaim! MDS Adapter Board. The eZ80F91 Module is mounted onto the eZ80Acclaim! MDS Adapter Board.

Kit Features

The key features of the eZ80F91 Modular Development Kit are:

- eZ80F91 Module:
  - eZ80F91 device operating at 50MHz, with 256KB of internal Flash memory, and 8KB of internal SRAM memory
  - 128KB of off-chip SRAM memory
  - On-chip Ethernet Media Access Controller (EMAC)
  - Ethernet port and PHY
  - Real-Time Clock support
  - Footprint for an SIR IrDA transceiver
  - Two 56-pin mini-module connectors for attachment to the eZ80Acclaim! MDS Adapter Board
- eZ80Acclaim! MDS Adapter Board:
  - Footprint for 2 M x 8 external Flash memory such as AM29LV160D
  - Footprint for 10-bit bus switch such as 74CBTLV3384, to support external Flash

  - RS-232 connector with interface circuit for UART0
  - ZDI and JTAG debug connectors
  - Two 56-pin mini-module connectors
  - Two 60-pin interface connectors for connection to an external application or development board (not supplied)
  - 32-pin header and footprint for a GPRS modem on UART1
  - One green 3.3 OK LED
  - One yellow Test LED and pushbutton
  - 5 VDC external power supply
- USB Smart Cable
- eZ80Acclaim! software and documentation CD-ROM
- Schematics for the eZ80F91 Mini Enet Module and eZ80Acclaim! MDS Adapter Board

Safeguards

The following precautions must be taken while working with the devices described in this document.

Caution: Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

eZ80F91 Modular Development Kit Overview

The purpose of the eZ80F91 Modular Development Kit is to provide a set of tools for designing an application based on the eZ80F91 microcontroller. A block diagram of the eZ80Acclaim! MDS Adapter Board is displayed in Figure 1 .

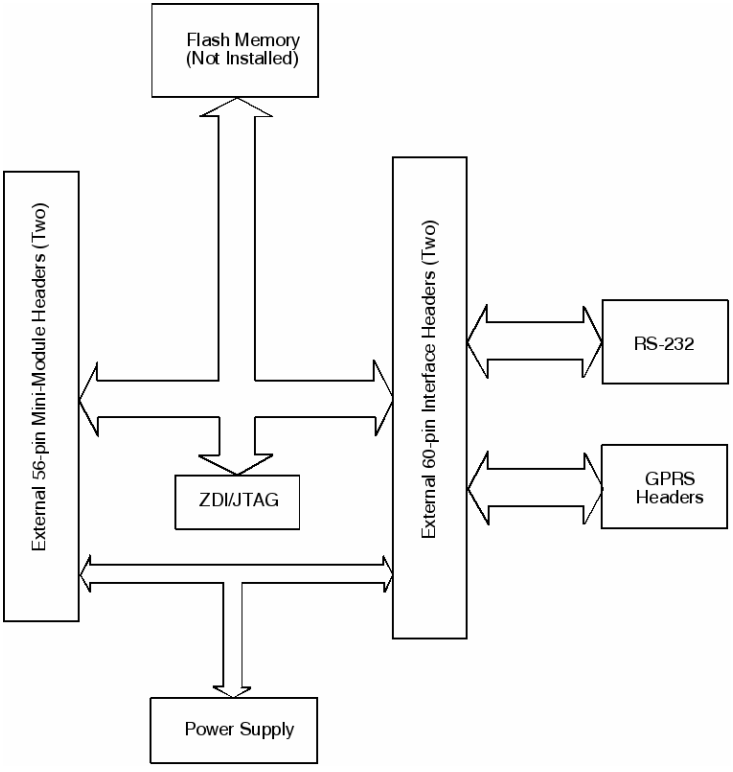


Figure 1. eZ80Acclaim! MDS Adapter Board Block Diagram

Figure 2 displays a block diagram of the eZ80F91 Module.

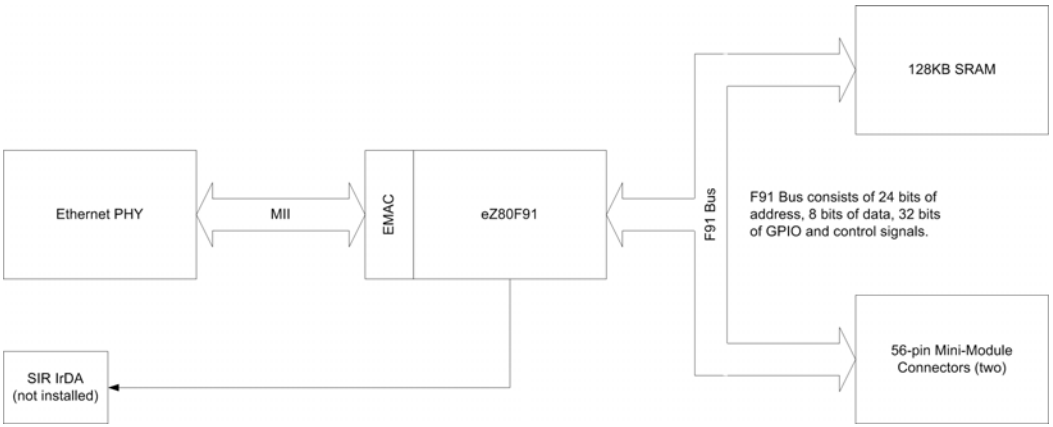


Figure 2. eZ80F91 Mini Enet Module Block Diagram

Schematics for the eZ80F91 Module and eZ80Acclaim! MDS Adapter Board are provided in the Schematics chapter on page 30.

eZ80Acclaim! MDS Adapter Board

This chapter describes the functions of the eZ80Acclaim! MDS Adapter Board.

eZ80F91 Module Interface

The eZ80F91 Module interface on the eZ80Acclaim! MDS Adapter Board consists of two 56-pin mini-module receptacles.

Almost all of these receptacles' signals are connected directly to the CPU. Three input signals offer options by disabling certain functions of the eZ80F91 Module.

These three input signals are:

Disable IrDA (DIS_IrDA). Used only if you have installed an external SIR IrDA transceiver onto the eZ80F91 Module. When the DIS_IrDA input signal is pulled Low, the IrDA transceiver located on the eZ80F91 Module is disabled. As a result, UART0 can be used with RS-232 or RS-485 interfaces on the eZ80 development platform.

F91_WE. When the F91_WE signal is active Low, internal Flash on the eZ80F91 chip is enabled for writing. This signal is inverted from the F91_WP signal on the eZ80F91 chip.

RTC_VDD. Test point for the Real-Time Clock power supply.

Peripheral Bus Mini-Module Connector J1

Figure 3 displays the pin layout of 56-pin Peripheral Bus Mini-Module Connector, J1, on the eZ80Acclaim! MDS Adapter Board. Table 1 lists the pins and their functions.

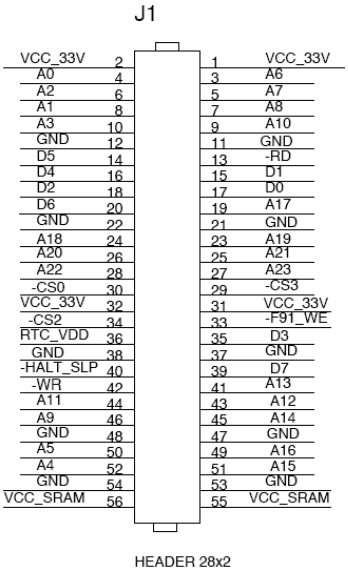


Figure 3. eZ80Acclaim! MDS Adapter Board Peripheral Bus Mini-Module Connector J1 Pin Configuration

Table 1. eZ80Acclaim! MDS Adapter Board Peripheral Bus Connector J1 Identification[1,2]

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal	Note
3	A6	Bidirectional	n/a	Yes	
4	A0	Bidirectional	n/a	Yes	

Notes:

1. To simplify the interface description, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS Adapter Board schematics; see Figures 8 and 9.
2. External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 MCU's Peripheral Power-Down Register.

Table 1. eZ80Acclaim! MDS Adapter Board Peripheral Bus Connector J1 Identification[1,2] (Continued)

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal	Note
5	A7	Bidirectional	n/a	Yes	
6	A2	Bidirectional	n/a	Yes	
7	A8	Bidirectional	n/a	Yes	
8	A1	Bidirectional	n/a	Yes	
9	A10	Bidirectional	n/a	Yes	
10	A3	Bidirectional	n/a	Yes	
13	RD	Output	Low	Yes	
14	D5	Bidirectional	n/a	Yes	
15	D1	Bidirectional	n/a	Yes	
16	D4	Bidirectional	n/a	Yes	
17	D0	Bidirectional	n/a	Yes	
18	D2	Bidirectional	n/a	Yes	
19	A17	Bidirectional	n/a	Yes	
20	D6	Bidirectional	n/a	Yes	
23	A19	Bidirectional	n/a	Yes	
24	A18	Bidirectional	n/a	Yes	
25	A21	Bidirectional	n/a	Yes	
26	A20	Bidirectional	n/a	Yes	
27	A23	Bidirectional	n/a	Yes	
28	A22	Bidirectional	n/a	Yes	

Notes:

1. To simplify the interface description, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS Adapter Board schematics; see Figures 8 and 9.
2. External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 MCU's Peripheral Power-Down Register.

Table 1. eZ80Acclaim! MDS Adapter Board Peripheral Bus Connector J1 Identification[1,2] (Continued)

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal	Note
29	CS3	Output	Low	Yes	
30	CS0	Output	Low	Yes	
33	F91_WE	Input	Low	No	Jumper on board
34	CS2	Output	Low	Yes	
35	D3	Bidirectional	n/a	Yes	
36	RTC_V_{DD}	Input	n/a	Yes	
39	D7	Bidirectional	n/a	Yes	
40	HALT_SLP	Output	Low	Yes	
41	A13	Bidirectional	n/a	Yes	
42	WR	Output	Low	Yes	
43	A12	Bidirectional	n/a	Yes	
44	A11	Bidirectional	n/a	Yes	
45	A14	Bidirectional	n/a	Yes	
46	A9	Bidirectional	n/a	Yes	
49	A16	Bidirectional	n/a	Yes	
50	A5	Bidirectional	n/a	Yes	
51	A15	Bidirectional	n/a	Yes	
52	A4	Bidirectional	n/a	Yes	

Notes:
1. To simplify the interface description, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS Adapter Board schematics; see Figures 8 and 9.
2. External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 MCU's Peripheral Power-Down Register.

I/O Mini-Module Connector J2

Figure 4 displays the pin layout of the 56-pin Peripheral Bus Mini-Module Connector, J2, on the eZ80Acclaim! MDS Adapter Board. Table 2 lists the pins and their functions.

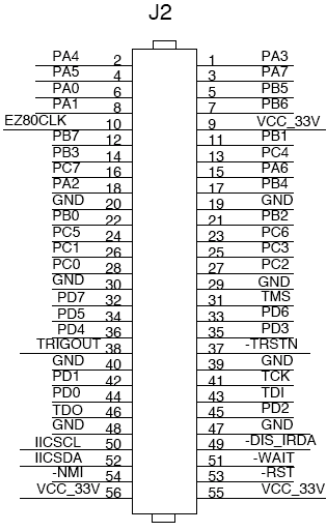


Figure 4. eZ80Acclaim! MDS Adapter Board I/O Mini-Module Connector J2

Table 2. eZ80Acclaim! MDS Adapter Board I/O Mini-Module Connector J2 Identification[1]

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1	PA3	Bidirectional	n/a	Yes
2	PA4	Bidirectional	n/a	Yes

Notes:
1. To simplify interface description, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS Adapter Board schematics; see Figures 8 and 9.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Table 2. eZ80Acclaim! MDS Adapter Board I/O Mini-Module Connector J2 Identification[1]

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
3	PA7	Bidirectional	n/a	Yes
4	PA5	Bidirectional	n/a	Yes
5	PB5	Bidirectional	n/a	Yes
6	PA0	Bidirectional	n/a	Yes
7	PB6	Bidirectional	n/a	Yes
8	PA1	Bidirectional	n/a	Yes
10	EZ80CLK	Output	n/a	Yes
11	PB1	Bidirectional	n/a	Yes
12	PB7	Bidirectional	n/a	Yes
13	PC4	Bidirectional	n/a	Yes
14	PB3	Bidirectional	n/a	Yes
15	PA6	Bidirectional	n/a	Yes
16	PC7	Bidirectional	n/a	Yes
17	PB4	Bidirectional	n/a	Yes
18	PA2	Bidirectional	n/a	Yes
21	PB2	Bidirectional	n/a	Yes
22	PB0	Bidirectional	n/a	Yes
23	PC6	Bidirectional	n/a	Yes
24	PC5	Bidirectional	n/a	Yes
25	PC3	Bidirectional	n/a	Yes
26	PC1	Bidirectional	n/a	Yes
27	PC2	Bidirectional	n/a	Yes

Notes:
1. To simplify interface description, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS Adapter Board schematics; see Figures 8 and 9.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Table 2. eZ80Acclaim! MDS Adapter Board I/O Mini-Module Connector J2 Identification[1]

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
28	PC0	Bidirectional	n/a	Yes
31	TMS	Input	n/a	Yes
32	PD7	Bidirectional	n/a	Yes
33	PD6	Bidirectional	n/a	Yes
34	PD5	Bidirectional	n/a	Yes
35	PD3	Bidirectional	n/a	Yes
36	PD4	Bidirectional	n/a	Yes
37	TRSTN	Input	Low	Yes
38	TRIGOUT	Output	n/a	Yes
41	TCK	Input	n/a	Yes
42	PD1	Bidirectional	n/a	Yes
43	TDI	Bidirectional	n/a	Yes
44	PD0	Bidirectional	n/a	Yes
45	PD2	Bidirectional	n/a	Yes
46	TDO	Output	n/a	Yes
49	DIS_IRDA	Input	Low	No
50	IICSCL	I/O	n/a	Yes
51	WAIT	Input	Low	Yes
52	IICSDA	I/O	n/a	Yes
53	RST	I/O	Low	Yes
54	NMI	Input	Low	Yes

Notes:
1. To simplify interface description, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS Adapter Board schematics; see Figures 8 and 9.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Peripheral and I/O External Interface

The Peripheral and I/O external interface on the eZ80Acclaim! MDS Adapter Board consists of two 60-pin mini-module receptacles.

Peripheral Bus External Connector JP1

Figure 5 displays the pin layout of Peripheral Bus External Connector, JP1, in the 60-pin header on the eZ80Acclaim! MDS Adapter Board. Table 3 lists the pins and their functions.

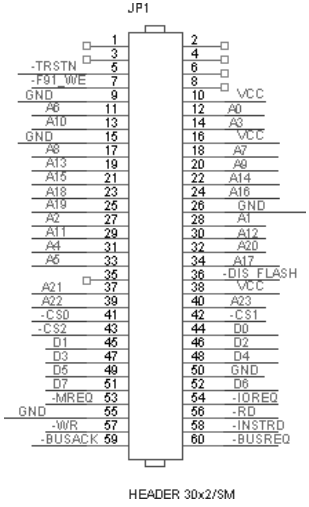


Figure 5. eZ80Acclaim! MDS Adapter Board Peripheral Bus External Connector JP1

Caution: The following signals are not connected and are unavailable on the associated pins:

- Pin 36, $\overline{\text{DIS\_FLASH}}$
- Pin 42, $\overline{\text{CS1}}$
- Pin 53, $\overline{\text{MREQ}}$
- Pin 54, $\overline{\text{IOREQ}}$
- Pin 58, $\overline{\text{INSTRD}}$
- Pin 59, $\overline{\text{BUSACK}}$
- Pin 60, $\overline{\text{BUSREQ}}$

Table 3. eZ80Acclaim! MDS Adapter Board Peripheral Bus External Connector JP1 Identification[1]

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1–4, 6, 8, 35	Unused	n/a	n/a	n/a
5	TRSTN	Input	Low	Yes
11	A6	Bidirectional	n/a	Yes
12	A0	Bidirectional	n/a	Yes
13	A10	Bidirectional	n/a	Yes
14	A3	Bidirectional	n/a	Yes
17	A8	Bidirectional	n/a	Yes
18	A7	Bidirectional	n/a	Yes

Notes:
1. To simplify interface description, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS Adapter Board schematics; see Figures 8 and 9.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Table 3. eZ80Acclaim! MDS Adapter Board Peripheral Bus External Connector JP1 Identification[1] (Continued)

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
19	A13	Bidirectional	n/a	Yes
20	A9	Bidirectional	n/a	Yes
21	A15	Bidirectional	n/a	Yes
22	A14	Bidirectional	n/a	Yes
23	A18	Bidirectional	n/a	Yes
24	A16	Bidirectional	n/a	Yes
25	A19	Bidirectional	n/a	Yes
27	A2	Bidirectional	n/a	Yes
28	A1	Bidirectional	n/a	Yes
29	A11	Bidirectional	n/a	Yes
30	A12	Bidirectional	n/a	Yes
31	A4	Bidirectional	n/a	Yes
32	A20	Bidirectional	n/a	Yes
33	A5	Bidirectional	n/a	Yes
34	A17	Bidirectional	n/a	Yes
36	DIS_FLASH	Input	Low	No
37	A21	Bidirectional	n/a	Yes
39	A22	Bidirectional	n/a	Yes
40	A23	Bidirectional	n/a	Yes
41	CS0	Output	Low	Yes
42	CS1	Output	Low	Yes
43	CS2	Output	Low	Yes

Notes:
1. To simplify interface description, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS Adapter Board schematics; see Figures 8 and 9.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Table 3. eZ80Acclaim! MDS Adapter Board Peripheral Bus External Connector JP1 Identification[1] (Continued)

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
44-49	D[0:5]	Bidirectional	n/a	Yes
51	D7	Bidirectional	n/a	Yes
52	D6	Bidirectional	n/a	Yes
53	MREQ	Output	Low	Yes
54	IOREQ	Output	Low	Yes
56	RD	Output	Low	Yes
57	WR	Output	Low	Yes
58	INSTRD	Output	Low	Yes
59	BUSACK	Output	Low	Yes
60	BUSREQ	Input	Low	Yes

Notes:
1. To simplify interface description, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS Adapter Board schematics; see Figures 8 and 9.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

I/O External Connector JP2

Figure 6 displays the pin layout of the I/O Connector in the 60-pin header on the eZ80Acclaim! MDS Adapter Board. Table 4 lists the pins and their functions.

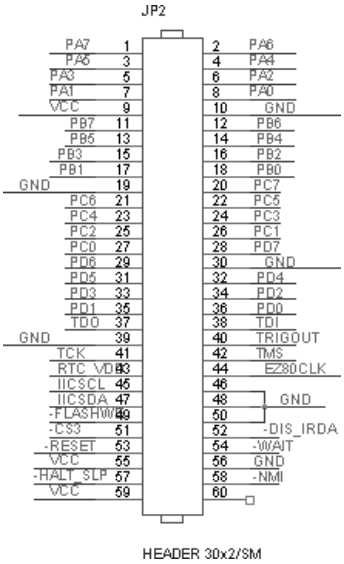


Figure 6. eZ80Acclaim! MDS Adapter Board I/O External Connector JP2

Caution: The $\overline{\text{FLASWE}}$ signal is disconnected and unavailable on pin 49.

Table 4. eZ80Acclaim! MDS Adapter Board I/O External Connector JP2 Identification[1]

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1–8	PA7 to PA0	Bidirectional	n/a	Yes
11–18	PB7 to PB0	Bidirectional	n/a	Yes
20–27	PC7 to PC0	Bidirectional	n/a	Yes
28, 29	PD7, PD6	Bidirectional	n/a	Yes
31–36	PD5 to PD0	Bidirectional	n/a	Yes
37	TDO	Output	n/a	Yes
38	TDI	I/O	n/a	Yes
40	TRIGOUT	Output	n/a	Yes
41	TCK	Input	n/a	Yes
42	TMS	Input	n/a	Yes
43	RTC_V_{DD}	Input	n/a	Yes
44	EZ80CLK	Output	n/a	Yes
45	IICSCL	I/O	n/a	Yes
47	IICSDA	I/O	n/a	Yes
49	FLASHWE	Input	Low	No
51	CS3	Output	Low	Yes
52	DIS_IRDA	Input	Low	No
53	RST	I/O	Low	Yes
54	WAIT	Input	Low	Yes
57	HALT_SLP	Output	Low	Yes
58	NMI	Input	Low	Yes
60	unused	n/a	n/a	n/a

Notes:
1. To simplify interface description, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS Adapter Board schematics; see Figures 8 and 9.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

GPRS Wireless Modem Interface

The MDS Adapter Board includes connectors for adding a MultiTech SocketModem GSM/GPRS data/fax wireless modem module, part numbers MTSMC-G-F1 (900/1800 MHz) or MTSMC-G-F2 (850/1900 MHz). This interface is implemented on the UART1 (PCx) interface and consists of connectors J3, J11, and J12. For information about the MultiTech module, refer to the Multitech website.

Figure 7 displays the pin layout of the three GPRS module connectors on the eZ80Acclaim! MDS Adapter Board. Table 5 lists connector J3 pins and functions. Table 6 lists connector J11 pins and functions.

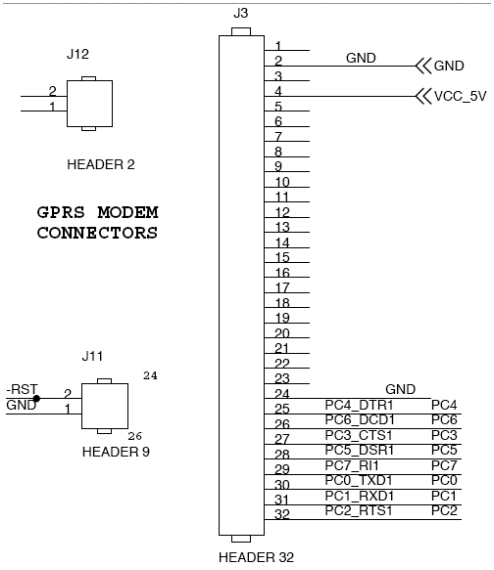


Figure 7. eZ80Acclaim! MDS Adapter Board GPRS Wireless Modem Connectors J3, J11 and J12

Note: The pins on Connector J12 are not connected to any MDS board signals.

Table 5. eZ80Acclaim! MDS Adapter Board GPRS Wireless Modem Connector J3 Identification

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal
1	unused	n/a	n/a	n/a
2	GND	n/a	n/a	Yes
3	unused	n/a	n/a	n/a
4	VCC_5V	n/a	n/a	No
5–23	unused	n/a	n/a	n/a
24	GND	n/a	n/a	Yes
25	PC4_DTR1	Output	Low	Yes
26	PC6_DCD1	Input	Low	Yes
27	PC3_CTS1	Input	Low	Yes
28	PC5_DSR1	Input	Low	Yes
29	PC7_RI1	Input	Low	Yes
30	PC0_TXD1	Output	n/a	Yes
31	PC1_RXD1	Input	n/a	Yes
32	PC2_RTS1	Output	Low	Yes

Table 6. eZ80Acclaim! MDS Adapter Board GPRS Wireless Modem Connector J11 Identification

Pin	Symbol	Signal Direction	Active Level	eZ80F91 Signal
1	RST	Output	Low	Yes
2	GND	n/a	n/a	Yes

eZ80Acclaim! MDS Adapter Board Jumper Settings

The eZ80Acclaim! MDS Adapter Board contains four jumpers that are listed in Table 7.

Table 7. eZ80Acclaim! MDS Adapter Board Jumper Settings

Jumper Name	Affected Device	Position	Function
J4, FL_EN	On-board Flash (when installed)	IN (Default)	On-board Flash is enabled.
		OUT	On-board Flash is disabled.
J6, FL_WEN[1]	On-board Flash (when installed)	IN	On-board Flash is disabled for writing.
		OUT	On-board Flash is enabled for writing
J8, RS-232-1 DIS	DB9 connector P2	IN	RS-232 output on connector P2 is disabled; PB6 = Don't Care.
		OUT	When PB 6 = 0, the RS-232 output on connector P2 is disabled. When PB 6 = 1, the RS-232 output on connector P2 is enabled. In all cases, the RS-232 input on connector P2 is enabled.
J9, IRDA_DIS[2]	IrDA transceiver (when installed)	IN (Default)	IrDA transceiver on eZ80F91 Mini Enet Module is disabled.
		OUT	IrDA transceiver on eZ80F91 Mini Enet Module is enabled.

Notes:
1. If AM29LV160 is used, J6 and R6 should be OUT. If AT49BV162 is used, R6 should be IN, and J6 should be OUT.
2. Jumper J9 functions only when you have installed IrDA transceiver on eZ80F91 Mini Enet Module.

eZ80Acclaim! MDS Adapter Board Test Switch and LEDs

The MDS Adapter Board contains a Test pushbutton switch (S1) and two LEDs (D1 and D2) that function as follows:

- Pressing the Test pushbutton S1 pulls PB3 Low
- The yellow LED, D1, is controlled by PB5 (active Low)
- The green LED, D2, is illuminated when power is applied to the board

eZ80F91 Module

This section describes the eZ80F91 Module hardware and its interfaces and key components, including the CPU, real-time clock and memory.

Functional Description

The eZ80F91 Module is a compact and high-performance module that has been designed for the rapid development and deployment of embedded systems. Despite its small footprint, the eZ80F91 Module provides a CPU, Ethernet interface, SRAM and real-time clock. This module is powered by the eZ80F91 microcontroller, a member of the eZ80Acclaim! product family.

eZ80F91 Module Operational Description

As a feature of the eZ80F91 Modular Development Kit, the purpose of the eZ80F91 Module is to provide a design platform to enable the use of such eZ80F91 device features as on-chip EMAC, SRAM and Flash.

Static RAM

The eZ80F91 Module features 128KB of fast SRAM. Access speed is typically 12ns, allowing zero-wait-state operation at 50MHz. With the CPU operating at 50MHz, SRAM can be accessed with zero wait states in eZ80 Mode. CS1_CTL ($\overline{CS1}$) can be set to `08h` (no wait states).

The eZ80F91 Mini Enet Module is shipped with SRAM powered from the same power supply as the eZ80F91 device. The SRAM can also be powered separately with a battery.

To power SRAM from a battery, observe the following brief procedure:

1. Remove R15.

2. Ensure that R14 is in place.
3. Connect the negative (–) battery lead to GND.
4. Connect the positive (+) battery lead to J10.

On-Chip Flash Memory

The eZ80F91 MCU on the eZ80F91 Module features 256KB of on-chip Flash memory, which can be programmed a single byte at a time, or in bursts of up to 256 bytes. Write operations can be performed using either memory or I/O instructions. Erasing bytes in Flash memory returns them to a value of FFh. Both the MASS ERASE and PAGE ERASE operations are self-timed by the Flash controller, leaving the CPU free to execute other operations in parallel. Upon power-up, on-chip Flash memory is located in the address range 000000h-03FFFFh. Four wait states are programmed in Flash Control Register F8h.

On-chip Flash memory is prioritized over all external chip selects, can be enabled or disabled (power-on enabled), and can be programmed within any 256KB address space in the 16MB address range.

The eZ80F91 Module features the following memory configurations:

- 8KB on-chip SRAM
- 128KB off-chip SRAM
- 256KB on-chip Flash

To learn more about the programming of internal Flash memory, refer to the eZ80F91 ASSP Product Specification (PS0270).

External Flash Memory

The eZ80F91 MDS Adapter Board provides a footprint for 2 MB of external Flash memory. The eZ80F91 Mini Enet Module supports this external

Flash via the full system bus, which is available on the expansion interface connectors.

PHY Circuit

The PHY KS8721 circuit has been extensively tested. However, for new designs, Zilog recommends that you refer to the following documentation on the Micrel website.

- KS8721BL/SL 3.3V Single Power Supply 10/100Base-TX/FX MII Physical Layer Transceiver Data Sheet
- KS8721BL/KS8721CL/KS8001L Design Guide for Interchangeability (Application Note 134)

IrDA Transceiver

The eZ80F91 Mini Enet Module is shipped without an IrDA transceiver installed. If you install an on-board transceiver, such as Zilog's ZHX1810, it connects to PD0 (TX), PD1 (RX) and PD2 (Shutdown, IR_SD). The IrDA transceiver is of the LED type 870nm Class 1. The IrDA transceiver is accessible via the IrDA Controller attached to UART0 on the eZ80F91 device.

To save power or to use the UART0 as a console, the transceiver can be disabled by the software or by an off-board signal when using the proper jumper selection. The transceiver is disabled by setting PD2 (IRDA_SD) High or by pulling the $\overline{\text{DIS\_IRDA}}$ pin on the I/O connector Low. The shutdown feature is used to save power. To enable the IrDA transceiver, $\overline{\text{DIS\_IRDA}}$ remains floating and PD2 is pulled Low.

The RxD and TxD signals on the transceiver perform the same functions as a standard RS-232 port. However, these signals are processed as IrDA 3/16 coding pulses (sometimes called IrDA encoder/decoder pulses). When the IrDA function is enabled, the final output to the RxD and TxD pins are routed through the 3/16 pulse generator.

Another signal that is used in the eZ80F91 Module's IrDA system is Shut_Down (SD). The SD pin is connected to PD2 on the eZ80F91 Module. The IrDA control software on the user's wireless device must enable this pin to wake the IrDA transceiver. The SD pin must be set Low to enable the IrDA transceiver. On eZ80F91 Module, a two-input OR gate is used to allow an external pin to shut down the IrDA transceiver. Both pins must be set Low to enable this function.

The eZ80F91 Module features an Infrared Encoder/Decoder register that configures the IrDA function. This register is located at address 0BFh in the internal I/O register map.

The Infrared Encoder/Decoder register contains three control bits:

Bit 0. Enables or disables the IrDA encoder/decoder block.

Bit 1. If set, this bit enables received data to pass into the UART0 Receive FIFO data buffer.

Bit 2. A test function that provides a loopback sequence from the TxD pin to the RxD input.

Bit 1, the Receive Enable bit, is used to block data from filling up the Receive FIFO when the eZ80F91 Module is transmitting data. Because air is the transmission medium that the the IrDA signal passes through, the transmitted data can also be received; the Receive Enable bit prevents this data from being received. After the eZ80F91 Module completes transmitting, this bit is changed to allow for incoming messages.

The code that follows provides an example of how this function is enabled on the eZ80F91 Module.

```
// Init_IRDA
// Make sure to first set PD2 as a port bit, an output and
// set it Low.

PD_ALT1 &= 0xFC;     // PD0 = uart0tx, PD1 = uart0_rx
PD_ALT2 |= 0x03;     // Enable alternate function
UART_LCTL0= 0x80;    // Select dlab to access baud rate
generator
BRG_DLRL0=0x2F;      // Baud rate Masterclock/(16*baudrate)
BRG_DLRH0=0x00;      // High byte of baud rate
UART_LCTL0=0x00;     // Disable dlab
UART_FCTL0=0xC7;     // Clear tx fifo, enable fifo
UART_LCTL0=0x03;     // 8bit, N, 1 stop
IR_CTL = 0x03;       // enable IRDA Encode/decode and Receive
                     // enable bit.
                     // IRDA_Xmit

IR_CTL = 0x01;       // Disable receive
Putchar(0xb0);       // Output a byte to the uart0 port.
```

Programming On-Chip Flash Memory

To program the 32 K boot block on the internal on-chip Flash memory, shunt JP1 on the eZ80F91 Mini Enet Module must be installed. Table 8 lists the settings for shunt JP1.

Table 8. Shunt JP1, eZ80F91 Module

Symbol	Jumper Name	Shunt Status	Function	Affected Device
JP1	F91_WE	In (Default)	On-chip Flash is enabled for writing to boot block.	On-chip Flash
		Out	On-chip Flash memory boot block is write-protected.	On-chip Flash

Note: Shunt JP2, labeled INT on the eZ80F91 Mini Enet Module schematic, is unpopulated. It is connected to pin 25 of the Ethernet PHY (KS8721) and can be used for test purposes.

Flash Loader Utility

The Flash Loader utility integrated within ZDSII allows a convenient way to program on-chip Flash memory. Refer to the Zilog Developer Studio II – eZ80Acclaim! User Manual (UM0144) for more details.

ZDSII

The Zilog Developer Studio II Integrated Development Environment (ZDSII IDE) is a complete stand-alone system that provides a state-of-the-art development environment. Based on the Windows Vista/Win 7/ WinXP Professional user interfaces, ZDSII integrates a language-sensitive editor, project manager, C Compiler, assembler, linker, librarian and source-level symbolic debugger that supports the eZ80F91 device.

For more information about ZDSII, refer to the Zilog Developer Studio II – eZ80Acclaim! User Manual (UM0144).

Troubleshooting

Before contacting Zilog Customer Support to submit a problem report, follow the simple steps outlined on this page. If a hardware failure is suspected, contact a local Zilog representative for assistance.

IrDA Port Not Working

If you are using the IrDA transceiver on the eZ80F91 Module, ensure that the hardware is set up as follows:

1. to enable the control gate that drives the IrDA device, turn OFF Jumper J9 on the eZ80Acclaim! MDS Adapter Board.
2. Set port pin PD2 Low. When this port pin and Jumper J9 are turned OFF, the IrDA device is enabled.
3. Disable the RS-232 output by installing a shunt on jumper J8 on the eZ80Acclaim! MDS Adapter Board.

Schematics

Figures 8 and 9 show schematic diagrams of the eZ80Acclaim! MDS Adapter Board. In these diagrams, Flash memory chip U2 is not installed; it is shown for reference only. When U2 is installed, it is accessed using CS3.

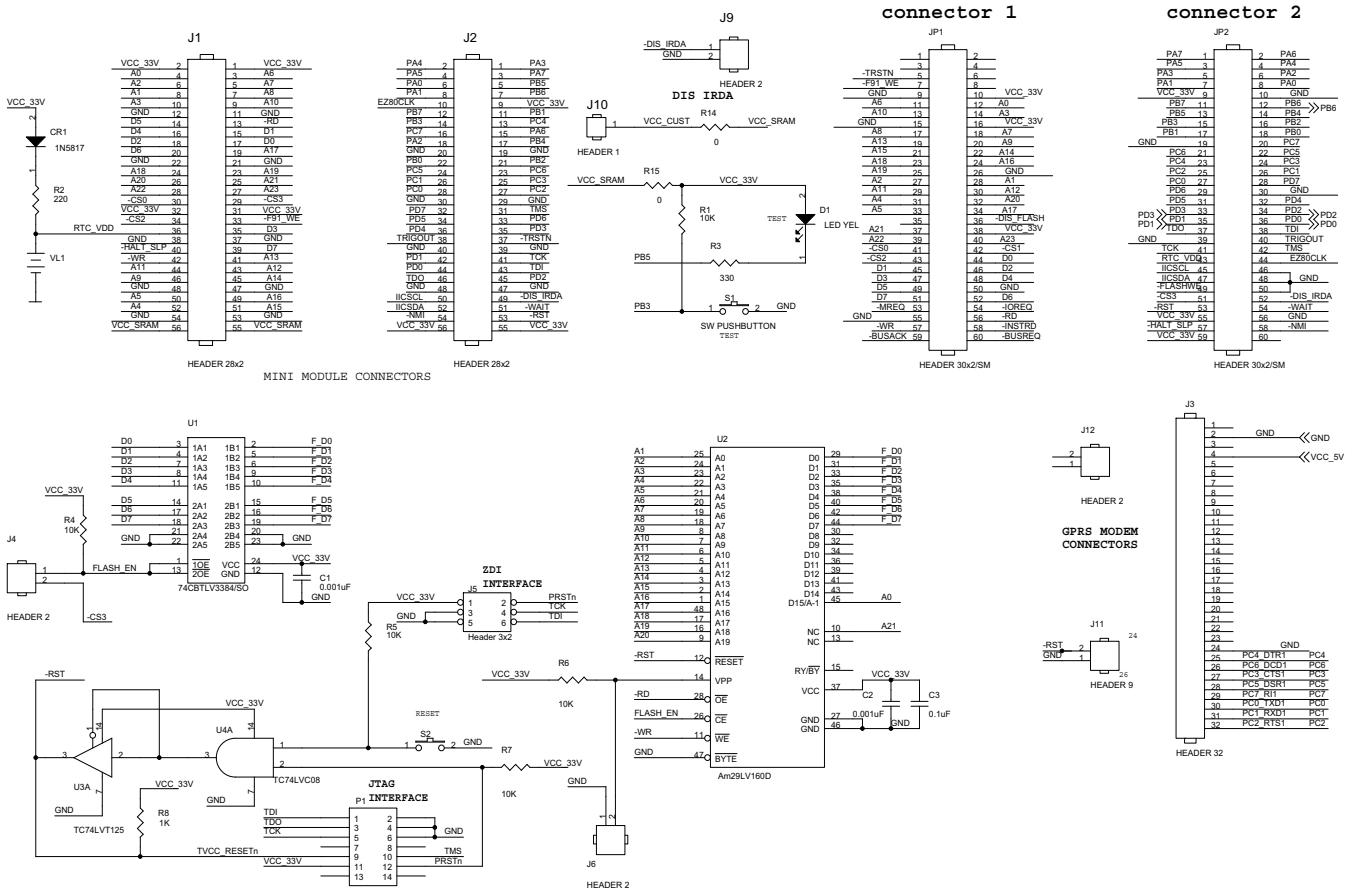


Figure 8. eZ80Acclaim! MDS B Schematic Diagram, #1 of 2

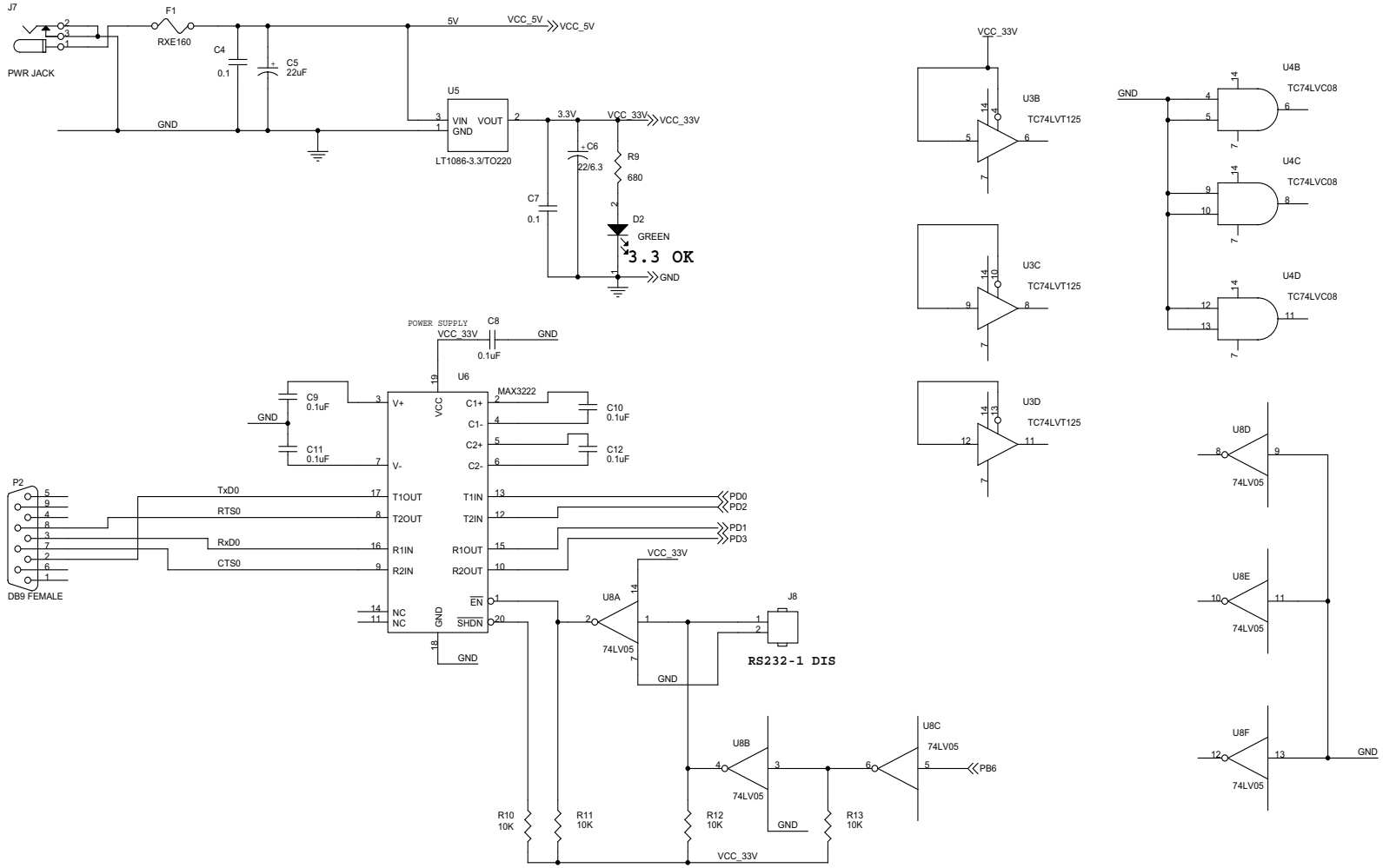


Figure 9. eZ80Acclaim! MDS Adapter Board Schematic, #2 of 2

Figures 10 and 11 show schematic diagrams of the eZ80F91 Module.

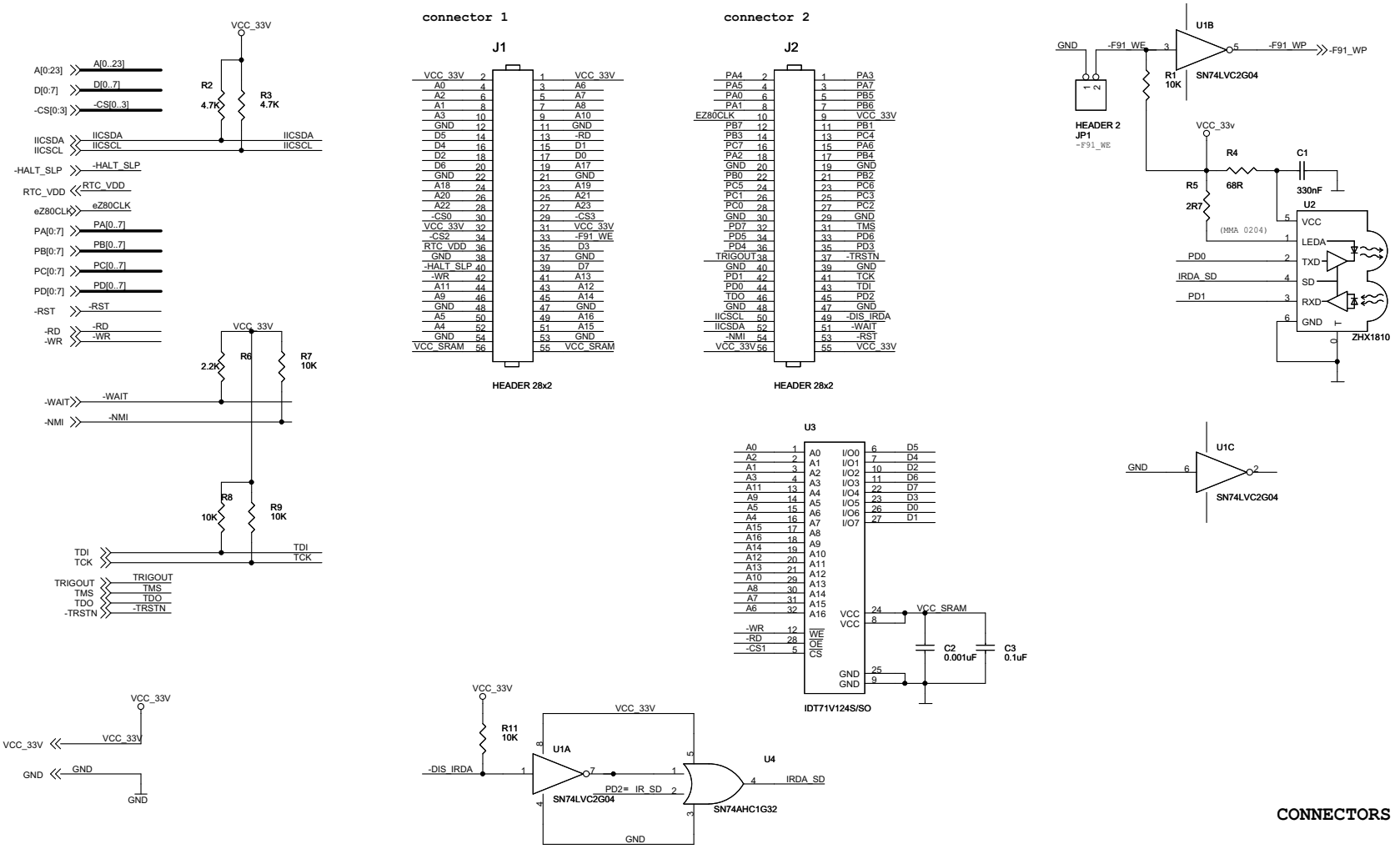


Figure 10. eZ80F91 Module Schematic, #1 of 2

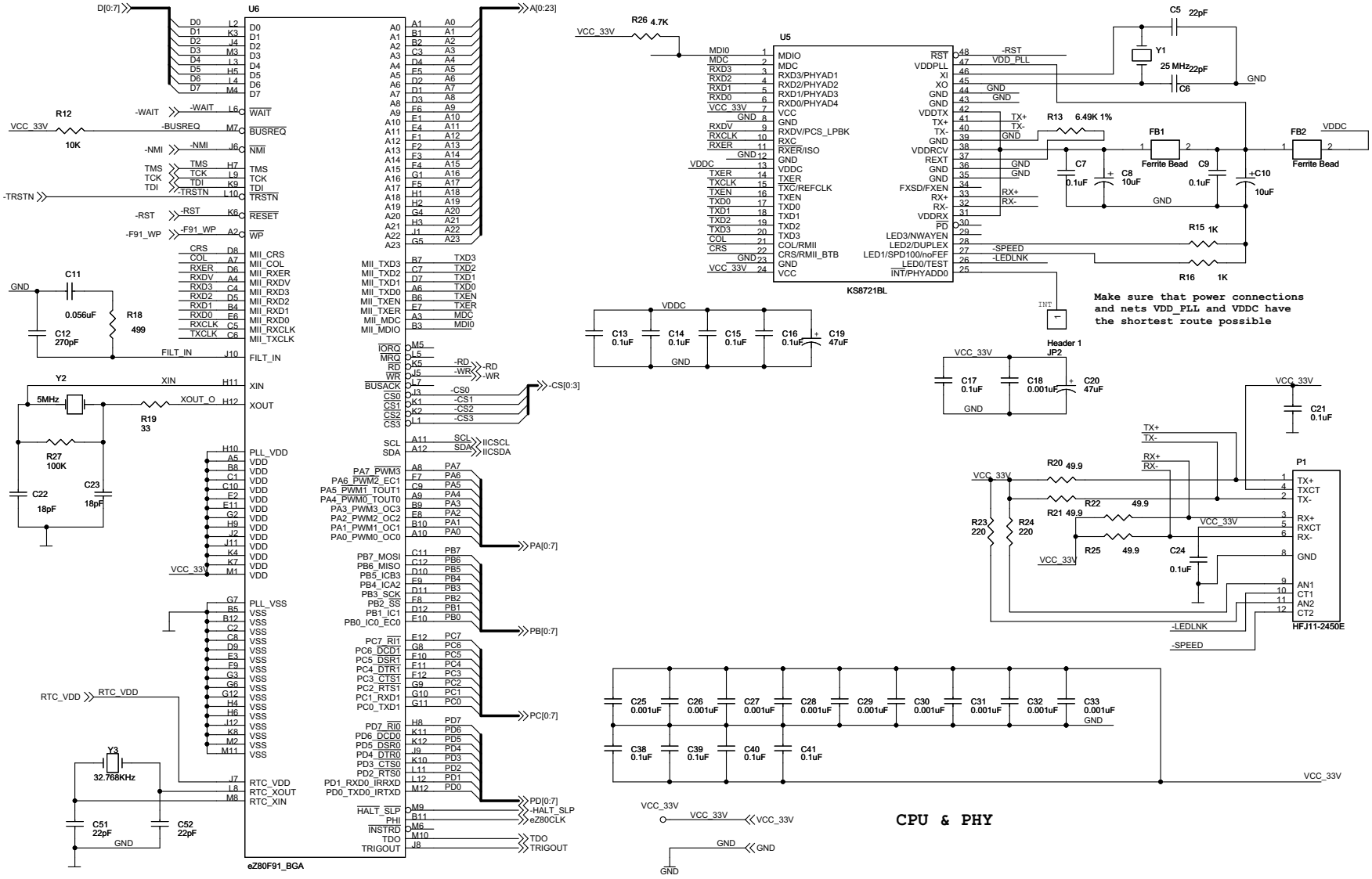
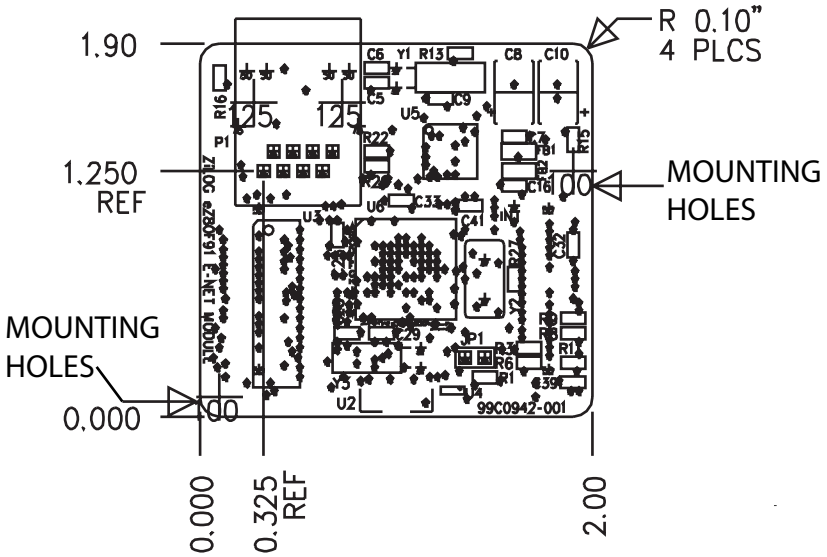


Figure 11. eZ80F91 Module Schematic, #2 of 2

Figure 12 indicates the physical dimensions of the eZ80F91 Ethernet Module.



HOLE SPECIFICATION			
SIZE	COUNT	SYMBOL	
.013	318	13	
.032	7	32	
.035	10	35	
.050	4	50	
.050	4	50	TOOL #40, UNPLATED
.075	2	75	
.100	2	100	
.125	2	125	

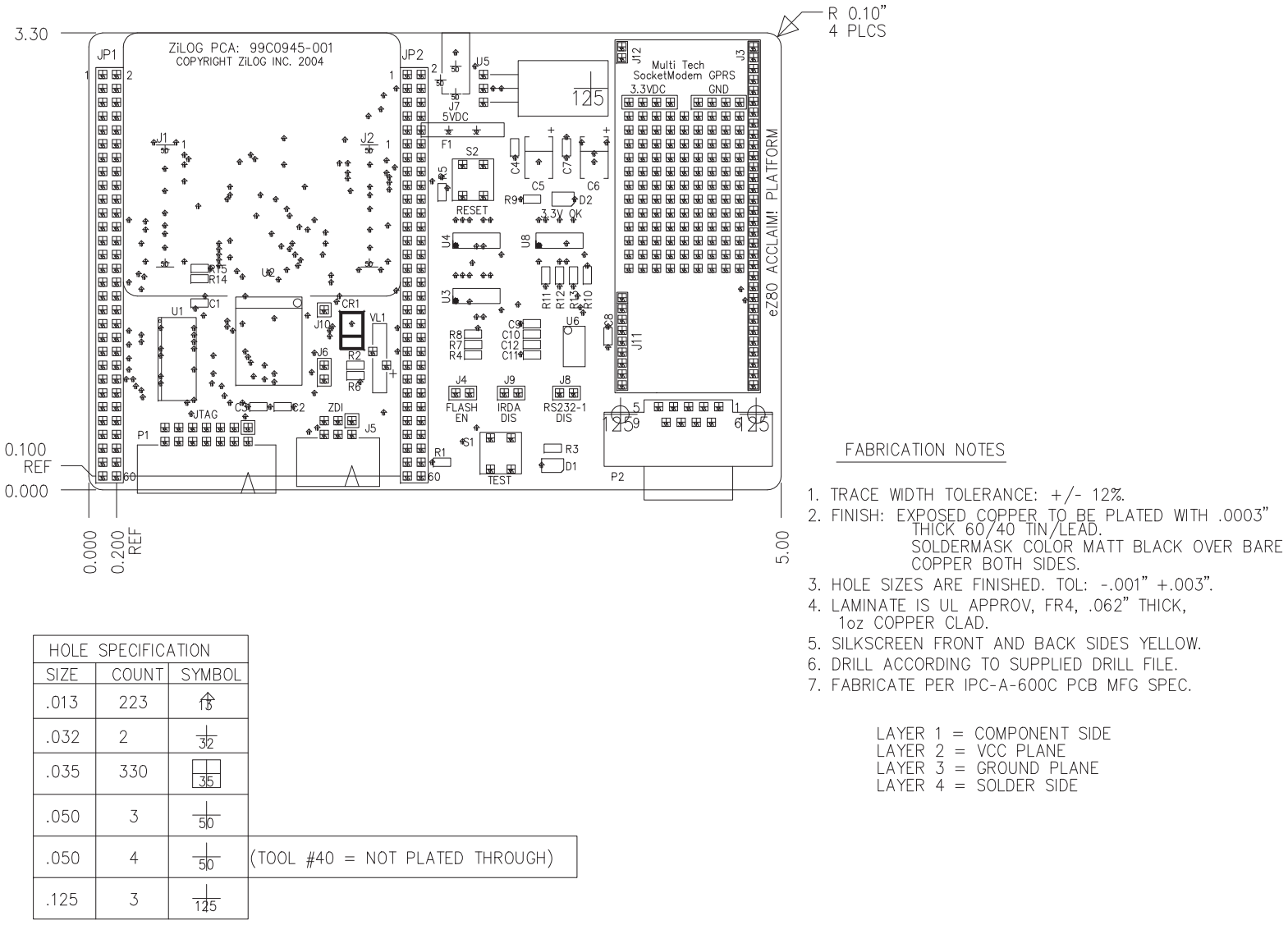
FABRICATION NOTES

1. TRACE WIDTH TOLERANCE: +/- 12%.
2. FINISH: EXPOSED COPPER TO BE PLATED WITH
   3-8 u INCH OF IMMERSION GOLD OVER
   150u INCHES ELECTROLESS NICKEL,
   PER IPC-4552
   SOLDERMASK COLOR MATT BLACK OVER BARE
   COPPER BOTH SIDES.
3. HOLE SIZES ARE FINISHED. TOL: -.001" +.003".
4. LAMINATE IS UL APPROV, FR4, .062" THICK,
   1oz COPPER CLAD.
5. SILKSCREEN BOTH SIDES YELLOW.
6. DRILL ACCORDING TO SUPPLIED DRILL FILE.
7. FABRICATE PER IPC-A-600C PCB MFG SPEC.

LAYER 1 = COMPONENT SIDE
LAYER 2 = INTERNAL SIGNAL #1
LAYER 3 = VCC PLANE
LAYER 4 = GROUND PLANE
LAYER 5 = INTERNAL SIGNAL #2
LAYER 6 = SOLDER SIDE

Figure 12. Physical Dimensions, eZ80F91 Ethernet Module

Figure 13 indicates the physical dimensions for the eZ80Acclaim! Platform.



HOLE SPECIFICATION		
SIZE	COUNT	SYMBOL
.013	223	13
.032	2	32
.035	330	35
.050	3	50
.050	4	50 (TOOL #40 = NOT PLATED THROUGH)
.125	3	125

FABRICATION NOTES

1. TRACE WIDTH TOLERANCE: +/- 12%.
2. FINISH: EXPOSED COPPER TO BE PLATED WITH .0003" THICK 60/40 TIN/LEAD. SOLDERMASK COLOR MATT BLACK OVER BARE COPPER BOTH SIDES.
3. HOLE SIZES ARE FINISHED. TOL: -.001" +.003".
4. LAMINATE IS UL APPROV, FR4, .062" THICK, 1oz COPPER CLAD.
5. SILKSCREEN FRONT AND BACK SIDES YELLOW.
6. DRILL ACCORDING TO SUPPLIED DRILL FILE.
7. FABRICATE PER IPC-A-600C PCB MFG SPEC.

LAYER 1 = COMPONENT SIDE
LAYER 2 = VCC PLANE
LAYER 3 = GROUND PLANE
LAYER 4 = SOLDER SIDE

Figure 13. Physical Dimensions, eZ80Acclaim! Development Platform

Customer Support

To share comments, get your technical questions answered, or report issues you may be experiencing with our products, please visit Zilog's Technical Support page at http://support.zilog.com.

To learn more about this product, find additional documentation, or to discover other facets about Zilog product offerings, please visit the Zilog Knowledge Base at http://zilog.com/kb or consider participating in the Zilog Forum at http://zilog.com/forum.

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