EiceDRIVER™ Compact

High voltage gate driver IC

6ED family - 2nd generation
Chip product

3 phase 600 V gate drive IC
6ED003L06-C2
6EDL04I06PC
6EDL04I06NC
6EDL04N06PC

EiceDRIVER™ Compact

datasheet

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all	revised wording of test temperature

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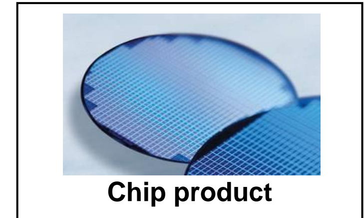
EiceDRIVER™ Compact
3 phase 600 V gate drive IC


Chip product

1 Overview

Main features

- Thin-film-SOI-technology
- Maximum blocking voltage +600V
- Separate control circuits for all six drivers
- CMOS and LSTTL compatible input (negative logic)
- Signal interlocking of every phase to prevent cross-conduction
- Detection of over current and under voltage supply
- externally programmable delay for fault clear after over current detection

Product highlights

- Insensitivity of the bridge output to negative transient voltages up to -50V given by SOI-technology
- Ultra fast bootstrap diodes (except 6ED003L06-C2)
- 'shut down' of all switches during error conditions

Typical applications

- Home appliances
- Fans, pumps
- General purpose drives

Product family

Table 1 Members of 6ED family – 2nd generation

Sales Name	high side control input HIN1,2,3 and LIN1,2,3	typ. UVLO-Thresholds	Bootstrap diode	Package	Replacement for 1st generation
6EDL04I06NC	negative logic	11.7 V / 9.8 V	Yes	sawn on foil	No
6EDL04I06PC	positive logic	11.7 V / 9.8 V	Yes	sawn on foil	No
6EDL04N06PC	positive logic	9 V / 8.1 V	Yes	sawn on foil	No
6ED003L06-C2	negative logic	11.7 V / 9.8 V	No	sawn on foil	Yes

Description

The device 6ED family – 2nd generation is a full bridge driver to control power devices like MOS-transistors or IGBTs in 3-phase systems with a maximum blocking voltage of +600 V. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch-up may occur at all temperatures and voltage conditions.

The six independent drivers are controlled at the low-side using CMOS resp. LSTTL compatible signals, down to 3.3 V logic. The device includes an under-voltage detection unit with hysteresis characteristic and an over-current detection. The over-current level is adjusted by choosing the resistor value and the threshold level at pin ITRIP. Both error conditions (under-voltage and over-current) lead to a definite shut down off all six switches. An error signal is provided at the FAULT open drain output pin. The blocking time after over-current can be adjusted with an RC-network at pin RCIN. The input RCIN owns an internal current source of 2.8 µA. Therefore, the resistor R_{RCIN} is optional. The typical output current can be given with 165 mA for pull-up and 375 mA for pull down. Because of system safety reasons a 310 ns interlocking time has been realised. The function of input EN

can optionally be extended with an over-temperature detection, using an external NTC-resistor (see Fig.1). The monolithic integrated bootstrap diode structures between pins VCC and VBx can be used for power supply of the high side.

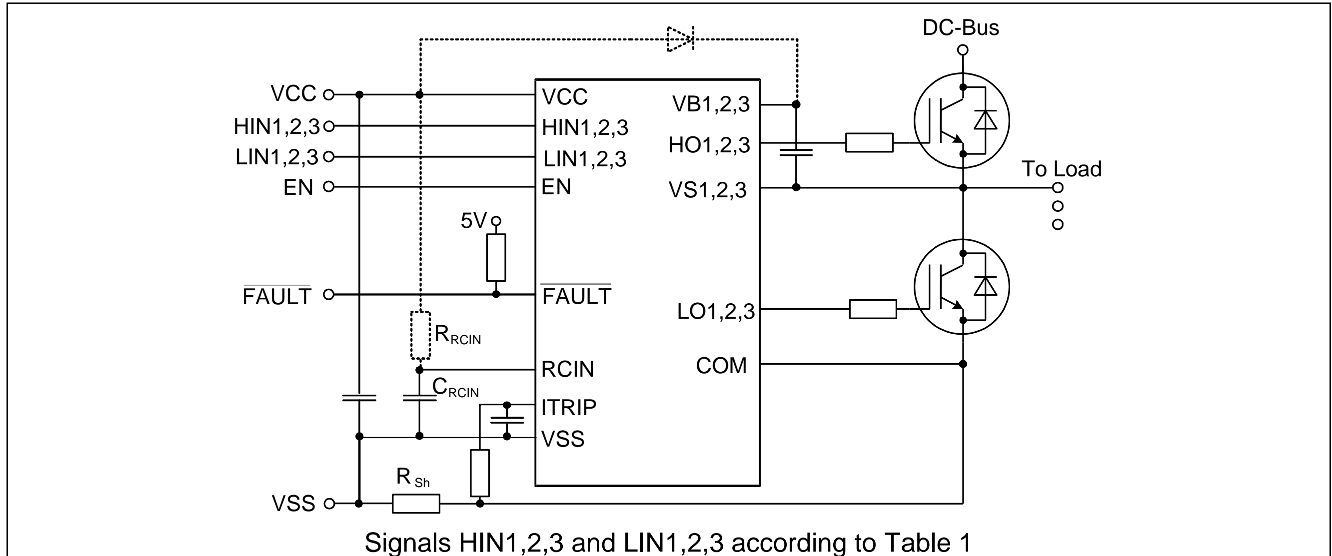


Figure 1 Typical Application

2 Blockdiagram

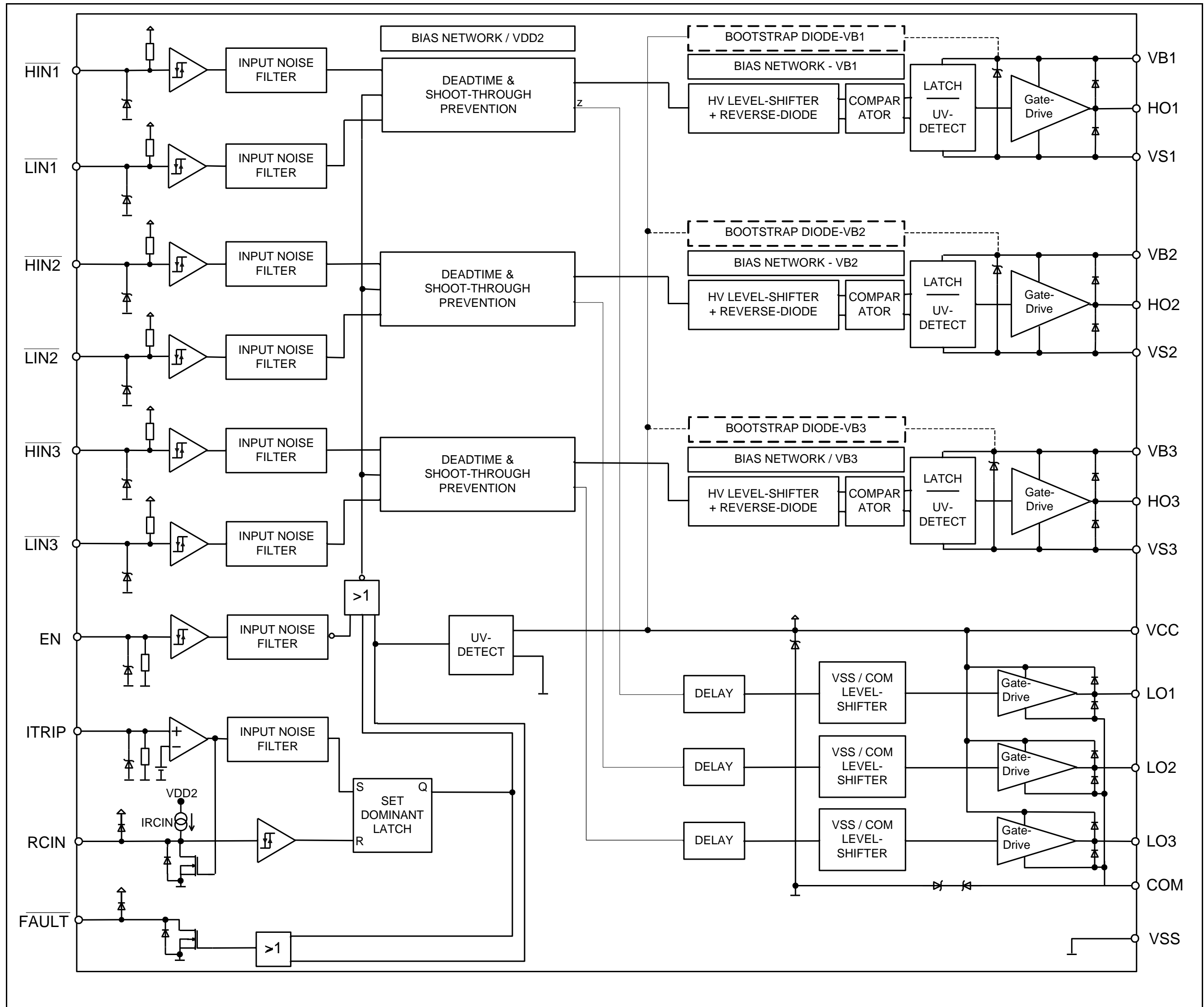


Figure 2 Block diagram for 6ED003L06-C2, and 6EDL04I06NC (with ultra fast BS diodes)

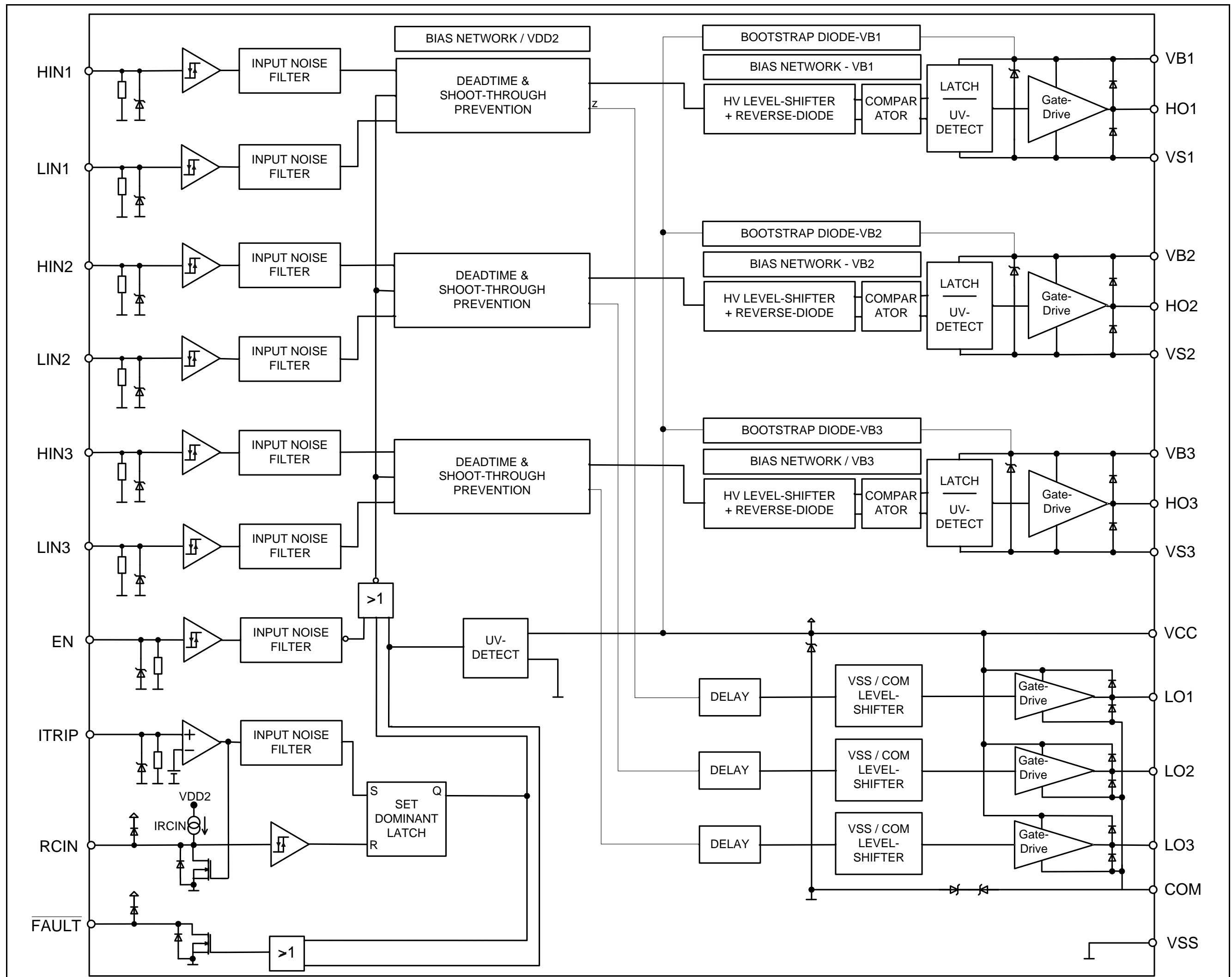


Figure 3 Block Diagram for 6EDL04I06PC, and 6EDL04N06PC

3 Chip size, bondpad configuration and description

3.1 Mechanical data

Table 2 Mechanical parameters

Raster size of die	2544 x 1706	µm x µm
Area total / active	4.34 / 4.65	mm²
Thickness	280	µm
Wafer size	200	mm
Max. possible chips per wafer	5908	pcs
Passivation frontside	Polyimide	
Backside (Note 2)	Grinded silicon	
Reject ink dot diameter	Min. 0.6 max 1.2	mm

Note1: Filler material inside the mould compound with sharp edges may harm the passivation.
Note2: Chip must be bonded onto an electrically isolated area

All pad openings are designed for gold wire ball bonds and not for aluminum wedge bonds.

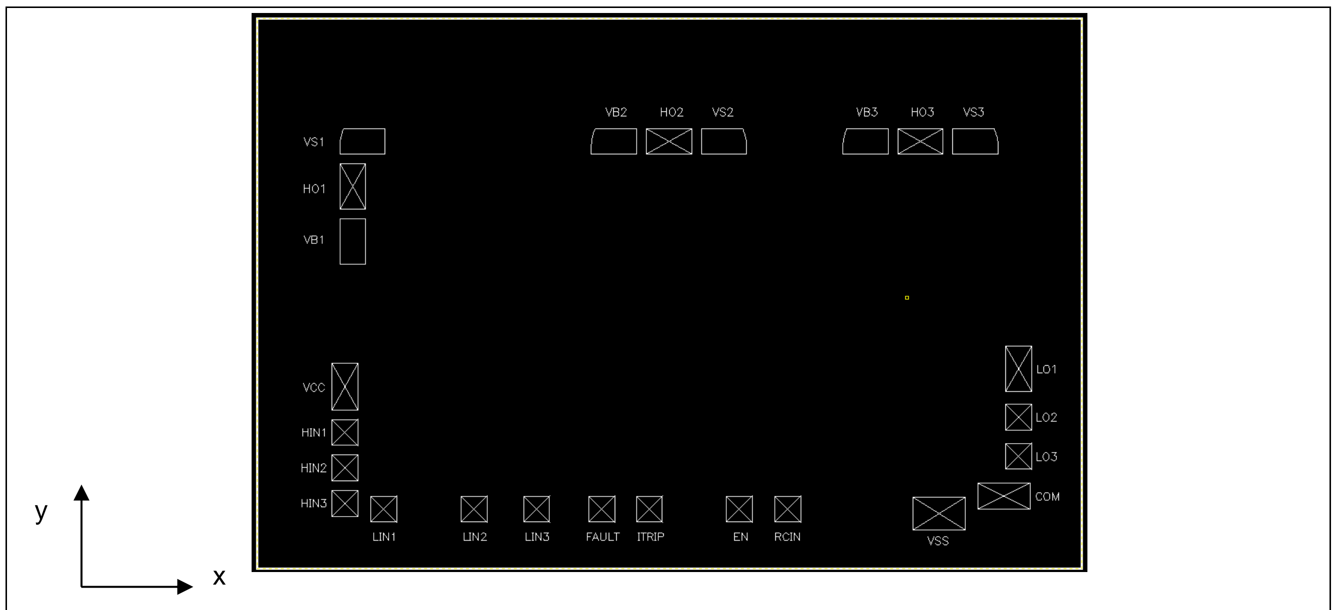


Figure 4 Bond pad configuration of 6ED family (signals HIN1,2,3 and LIN1,2,3 according to Table 1)

Table 3 Pad position and dimension

Pad Name	Pad Number	Voltage Domain	Pad Center Coordinates /µm		Active Pad Dimension /µm	
			X	Y	X	Y
VCC	1	1	271	565	80	145
HIN1	2	1	271	423	80	80
HIN2	3	1	271	313	80	80
HIN3	4	1	271	203	80	80
LIN1	5	1	390	185	80	80
LIN2	6	1	669	185	80	80

Table 3 Pad position and dimension

Pad Name	Pad Number	Voltage Domain	Pad Center Coordinates /µm		Active Pad Dimension /µm	
			X	Y	X	Y
LIN3	7	1	862	185	80	80
FAULT	8	1	1063	185	80	80
ITRIP	9	1	1210	185	80	80
EN	10	1	1488	185	80	80
RCIN	11	1	1637	185	80	80
VSS	12	1	2104	171	160	100
COM	13	1	2305	226	160	80
LO3	14	1	2350	349	80	80
LO2	15	1	2350	469	80	80
LO1	16	1	2350	619	80	140
VS3	18	2	2217	1325	140	80
HO3	19	2	2047	1325	140	80
VB3	20	2	1877	1325	140	80
VS2	22	3	1440	1325	140	80
HO2	23	3	1270	1325	140	80
VB2	24	3	1100	1325	140	80
VS1	26	4	324	1325	140	80
HO1	27	4	294	1185	80	140
VB1	28	4	294	1014	80	140
Chip back side	---	floating	---	---	---	---

3.2 Pad description

Table 4 Pad Description

Symbol	Description
VCC	Low side power supply
VSS	Logic ground
/HIN1,2,3	High side logic input (negative logic)
/LIN1,2,3	Low side logic input (negative logic)
/FAULT	Indicates over-current and under-voltage (negative logic, open-drain output)
EN	Enable I/O functionality (positive logic)
ITRIP	Analog input for over-current shutdown, activates FAULT and RCIN to VSS
RCIN	external RC-network to define FAULT clear delay after FAULT-Signal (T_{FLTCLR})
COM	Low side gate driver reference
VB1,2,3	High side positive power supply
HO1,2,3	High side gate driver output
VS1,2,3	High side negative power supply
LO1,2,3	Low side gate driver output
Chip back side	Floating back side (floats towards the highest momentarily active potential)

3.3 Low Side and High Side Control Pins (Pin 2, 3, 4, 5, 6, 7)

The Schmitt trigger input threshold of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Input Schmitt trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 5 and Figure 6.

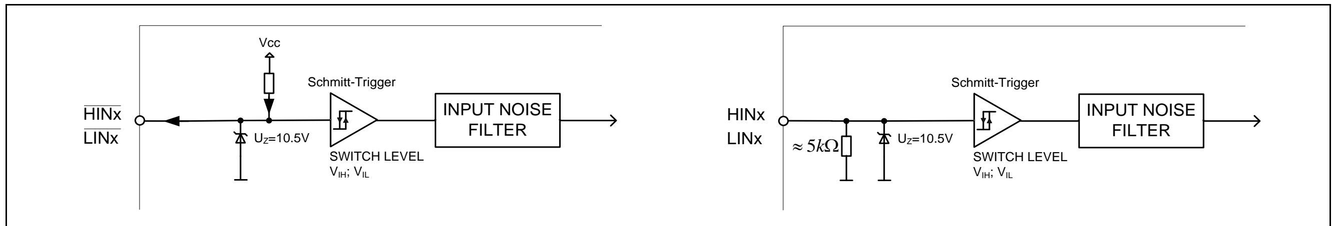


Figure 5 Input pin structure for negative logic (left) and positive logic (right)

An internal pull-up of about 75 kΩ (negative logic) pre-biases the input during supply start-up and a ESD zener clamp is provided for pin protection purposes. The zener diodes are therefore designed for single pulse stress only and not for continuous voltage stress over 10V. For versions with positive, a 5 kΩ pull-down resistor is used for this function.

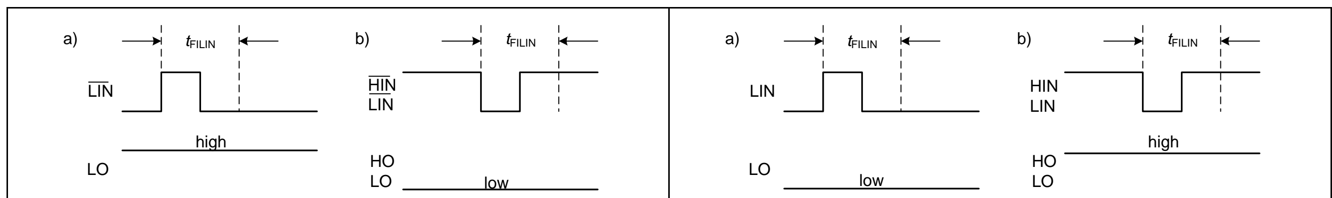


Figure 6 Input filter timing diagram for negative logic (left) and positive logic (right)

It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 1 µs.

The 6ED family – 2nd generation provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two channels of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only one leg output is activated, so that the leg is kept steadily in a safe state. Please refer to the application note AN-Gatedrive-6ED2-1 for a detailed description.

A minimum dead time insertion of typ. 310 ns is also provided, in order to reduce cross-conduction of the external power switches.

3.4 EN (Gate Driver Enable, Pin 10)

The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. The internal structure of the pin is given in Figure 7. The switching levels of the Schmitt-Trigger are here $V_{EN,TH+}$ = 2.1 V and $V_{EN,TH-}$ = 1.3 V. The typical propagation delay time is t_{EN} = 780 ns. There is an internal pull down resistor (75 kΩ), which keeps the gate outputs off in case of broken PCB connection.

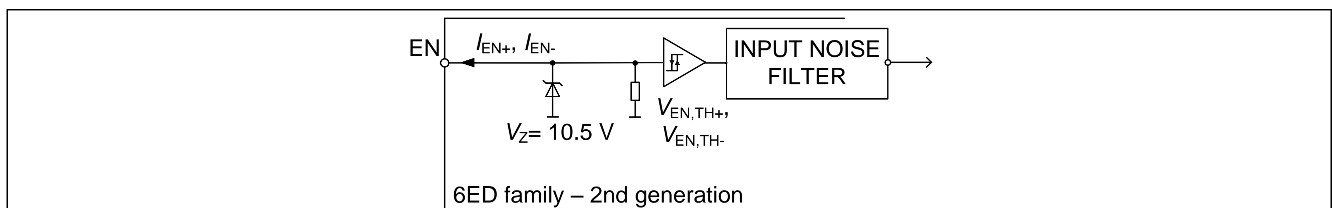


Figure 7 EN pin structures

3.5 /FAULT (Fault Feedback, Pin 8)

/Fault pin is an active low open-drain output indicating the status of the gate driver (see Figure 8). The pin is active (i.e. forces LOW voltage level) when one of the following conditions occur:

- Under-voltage condition of VCC supply: In this case the fault condition is released as soon as the supply voltage condition returns in the normal operation range (please refer to VCC pin description for more details).
- Over-current detection (ITRIP): The fault condition is latched until current trip condition is finished and RCIN input is released (please refer to ITRIP pin).

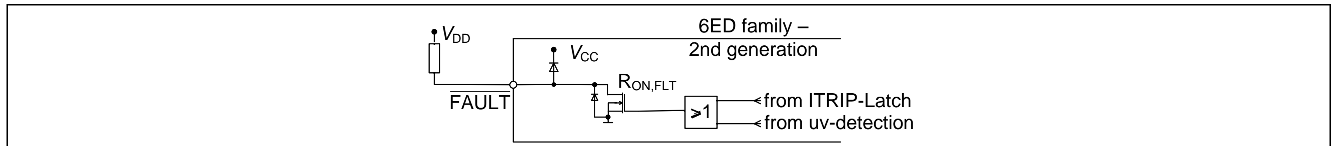


Figure 8 /FAULT pin structures

3.6 ITRIP and RCIN (Over-Current Detection Function, Pin 9, 11)

The 6ED family – 2nd generation provides an over-current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ 0.44 V) is referenced to VSS ground. A input noise filter (typ. $t_{ITRIPMIN}$ = 230 ns) prevents the driver to detect false over-current events.

Over-current detection generates a hard shut down of all outputs of the gate driver and provides a latched fault feedback at /FAULT pin. RCIN input/output pin is used to determine the reset time of the fault condition. As soon as ITRIP threshold is exceeded the external capacitor connected to RCIN is fully discharged. The capacitor is then recharged by the RCIN current generator when the over-current condition is finished. As soon as RCIN voltage exceeds the rising threshold of typ $V_{RCIN,TH}$ = 5.2 V, the fault condition releases and the driver returns operational following the ontrol input pins according to section 3.3. Please refer to AN-Gatedrive-6ED2-1 for details on setting RCIN time constant.

3.7 VCC, VSS and COM (Low Side Supply, Pin 1, 12,13)

VCC is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit. Output power stage is referenced to COM ground. COM ground is floating respect to VSS ground with a maximum range of operation of +/-5.7 V. A back-to-back zener structure protects grounds from noise spikes.

The under-voltage circuit enables the device to operate at power on when a typical supply voltage higher than V_{CCUV+} is present. The IC shuts down all the gate drivers power outputs, when the VCC supply voltage is below V_{CCUV-} = 9.8 V respectively 8.1 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

3.8 VB1,2,3 and VS1,2,3 (High Side Supplies, Pin 18, 20, 22, 24, 26, 28)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter/source voltage. Due to the low power consumption, the floating driver stage can be supplied by bootstrap topology connected to VCC.

The device operating area as a function of the supply voltage is given in Figure 15 and Figure 16. Details on bootstrap supply section and transient immunity can be found in application note AN-Gatedrive-6ED2-1.

3.9 LO1,2,3 and HO1,2,3 (Low and High Side Outputs, Pin 14, 15, 16, 19, 23, 27)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive of IGBT and MOSFET devices. Low side outputs (i.e. LO1,2,3) are state triggered by the respective inputs, while high side outputs (i.e. HO1,2,3) are edge triggered by the respective inputs. In particular, after an under voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after a under voltage condition of the VCC supply, the low side outputs switch to the state of their respective inputs.

4 Electrical Parameters

4.1 Absolute Maximum Ratings

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 5 Abs. maximum ratings

Parameter	Symbol	Min.	Max.	Unit
High side offset voltage(Note 1)	V_S	V_{CC}-V_{BS}-6	600	V
High side offset voltage (t_p<500ns, Note 1)		V_{CC} -V_{BS} – 50	–	
High side offset voltage(Note 1)	V_B	V_{CC} – 6	620	
High side offset voltage (t_p<500ns, Note 1)		V_{CC} – 50	–	
Chip back side	V_{Back}	V_{CC}-V_{BS}-6	620	
High side floating supply voltage (V_B vs. V_S) (internally clamped)		-1	20	
High side output voltage (V_{HO} vs. V_S)	V_{HO}	-0.5	V_B + 0.5	
Low side supply voltage (internally clamped)	V_{CC}	-1	20	
Low side supply voltage (V_{CC} vs. V_{COM})	V_{CCOM}	-0.5	25	
Gate driver ground	V_{COM}	-5.7	5.7	
Low side output voltage (V_{LO} vs. V_{COM})	V_{LO}	-0.5	V_{CCOM} + 0.5	
Input voltage LIN,HIN,EN,ITRIP	V_{IN}	-1	10	
FAULT output voltage	V_{FLT}	-0.5	V_{CC} + 0.5	
RCIN output voltage	V_{RCIN}	-0.5	V_{CC} + 0.5	
Junction temperature	T_J	–	125	°C
Storage temperature	T_S	- 40	150	
offset voltage slew rate	dV_S/dt		50	V/ns

Note :The minimum value for ESD immunity is 1.0kV (Human Body Model). ESD immunity inside pins connected to the low side (VCC, HINx, LINx, FAULT, EN, RCIN, ITRIP, VSS, COM, LOx) and pins connected inside each high side itself (VBx, HOx, VSx) is guaranteed up to 1.5kV (Human Body Model).

Note 1 : In case V_{CC} > V_B there is an additional power dissipation in the internal bootstrap diode between pins VCC and VBx. Insensitivity of bridge output to negative transient voltage up to –50V is not subject to production test – verified by design / characterization.

4.2 Required operation conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 6 Required Operation Conditions

Parameter	Symbol	Min.	Max.	Unit
High side offset voltage (Note 1)	V_B	7	620	V
Low side supply voltage (V_{CC} vs. V_{COM})	V_{CCOM}	10	25	

4.3 Operating Range

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 7 Operating range

Parameter		Symbol	Min.	Max.	Unit
High side floating supply offset voltage		V_S	V_{CC} - V_{BS} -1	550	V
High side floating supply offset voltage (V_B vs. V_{CC}, statically)		V_{BCC}	-1.0	550	
High side floating supply voltage (V_B vs. V_S, Note 1)	6EDL04I06NC 6EDL04I06PC 6ED003L06-C2	V_{BS}	13	17.5	
	6EDL04N06PC				
High side output voltage (V_{HO} vs. V_S)		V_{HO}	10	V_{BS}	
Low side output voltage (V_{LO} vs. V_{COM})		V_{LO}	0	V_{CC}	
Low side supply voltage	6EDL04I06NC 6EDL04I06PC 6ED003L06-C2	V_{CC}	13	17.5	
	6EDL04N06PC		10	17.5	
Low side ground voltage		V_{COM}	-2.5	2.5	
Logic input voltages LIN,HIN,EN,ITRIP (Note 2)		V_{IN}	0	5	
FAULT output voltage		V_{FLT}	0	V_{CC}	
RCIN input voltage		V_{RCIN}	0	V_{CC}	
Pulse width for ON or OFF (Note 3)		t_{IN}	1	–	µs
Ambient temperature		T_a	-40	95	°C

Note 1 : Logic operational for V_B (V_B vs. V_S) > 7,0V

Note 2 : All input pins (HINx, LINx) and EN, ITRIP pin are internally clamped (see abs. maximum ratings)

Note 3 : In case of input pulse width at LINx and HINx below 1µ the input pulse may not be transmitted properly

4.4 Static logic function table

VCC	VBS	RCIN	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<V_{CCUV-}	X	X	X	X	0	0	0
15V	<V_{BSUV-}	X	0	3.3 V	High imp	LIN1,2,3*	0
15V	15V	<3.2 V ↓	0	3.3 V	0	0	0
15V	15V	X	> $V_{IT,TH+}$	3.3 V	0	0	0
15V	15V	> $V_{RCIN,TH}$	0	3.3 V	High imp	LIN1,2,3*	HIN1,2,3*
15V	15V	> $V_{RCIN,TH}$	0	0	High imp	0	0

* according to Table 1

4.5 Static parameters

V_{CC} = V_{BS} = 15V unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 8 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
High level input voltage		V_{IH}	1.7	2.1	2.4	V	
Low level input voltage		V_{IL}	0.7	0.9	1.1		
EN positive going threshold		$V_{EN,TH+}$	1.9	2.1	2.3		
EN negative going threshold		$V_{EN,TH-}$	1.1	1.3	1.5		
ITRIP positive going threshold		$V_{IT,TH+}$	380	445	510	mV	
ITRIP input hysteresis		$V_{IT,HYS}$	45	70			
RCIN positive going threshold		$V_{RCIN,TH}$	-	5.2	6.4	V	
RCIN input hysteresis		$V_{RCIN,HYS}$	-	2.0	-		
Input clamp voltage (HIN and LIN acc. Table 1, EN, ITRIP)		$V_{IN,CLMAP}$	9	10.3	12		I_{IN} = 4mA
Input clamp voltage at high impedance (/HIN, /LIN negative logic only)		$V_{IN,FLOAT}$	-	5.3	5.8		controller output pin floating
High level output voltage	LO1,2,3 HO1,2,3	V_{OH}	- -	V_{CC} -0.7 V_B -0.7	V_{CC} -1.4 V_B -1.4		I_O = 20mA
Low level output voltage	LO1,2,3 HO1,2,3	V_{OL}	- -	V_{COM}+ 0.2 V_S+ 0.2	V_{COM}+ 0.6 V_S + 0.6		I_O = -20mA
V_{CC} and V_{BS} supply undervoltage positive going threshold	6EDL04I06NC 6EDL04I06PC 6ED003L06-C2	V_{CCUV+} V_{BSUV+}	11	11.7	12.5		
	6EDL04N06PC		8.3	9	9.8		
V_{CC} and V_{BS} supply undervoltage negative going threshold	6EDL04I06NC 6EDL04I06PC 6ED003L06-C2	V_{CCUV-} V_{BSUV-}	9.5	9.8	10.8	V	
	6EDL04N06PC		7.5	8.1	8.8		

Table 8 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
V_{CC} and V_{BS} supply undervoltage lockout hysteresis	6EDL04I06NC 6EDL04I06PC 6ED003L06-C2	V_{CCUVH} V_{BSUVH}	1.2	1.9	-		
	6EDL04N06PC		0.5	0.9	-		
High side leakage current betw. VS and VSS		I_{LVS+}	-	1	12.5	µA	V_S = 600V
High side leakage current betw. VS and VSS		I_{LVS+} [1]	-	10	-		T_J = 125°C, V_S = 600V
High side leakage current between VSx and VSy (x=1,2,3 and y=1,2,3)		I_{LVS-} [1]	-	10	-		T_J = 125°C V_{Sx} - V_{Sy} = 600V
Quiescent current V_{BS} supply (VB only)		I_{QBS1}	-	210	400	µA	HO=low
Quiescent current V_{BS} supply (VB only)		I_{QBS2}	-	210	400		HO=high
Quiescent current V_{CC} supply (VCC only)	6EDL04I06NC 6ED003L06-C2	I_{QCC1}	-	1.1	1.8	mA	V_{LIN}=float.
	6EDL04I06PC 6EDL04N06PC		-	0.75	1.5		
Quiescent current V_{CC} supply (VCC only)	6EDL04I06NC 6ED003L06-C2	I_{QCC2}	-	1.3	2		V_{LIN}=0, V_{HIN}=3.3 V
	6EDL04I06PC 6EDL04N06PC			0.75	1.5		V_{LIN}=3.3 V, V_{HIN}=0
Quiescent current V_{CC} supply (VCC only)	6EDL04I06NC 6ED003L06-C2	I_{QCC3}	-	1.3	2		V_{LIN}=3.3 V, V_{HIN}=0
	6EDL04I06PC 6EDL04N06PC			0.75	1.5		V_{LIN}=3.3 V, V_{HIN}=0
Input bias current	6EDL04I06NC 6ED003L06-C2	I_{LIN+}	-	70	100	µA	V_{LIN}=3.3 V
	6EDL04I06PC 6EDL04N06PC		400	700	1100		
Input bias current	6EDL04I06NC 6ED003L06-C2	I_{LIN-}	-	110	200	µA	V_{LIN}=0
	6EDL04I06PC 6EDL04N06PC			0			
Input bias current	6EDL04I06NC 6ED003L06-C2	I_{HIN+}	-	70	100		V_{HIN}=3.3 V
	6EDL04I06PC 6EDL04N06PC		400	700	1100		
Input bias current	6EDL04I06NC 6ED003L06-C2	I_{HIN-}	-	110	200		V_{HIN}=0
	6EDL04I06PC 6EDL04N06PC			0			
Input bias current (ITRIP=high)		I_{ITRIP+}		45	120		V_{ITRIP}=3.3 V
Input bias current (EN=high)		I_{EN+}	-	45	120		V_{ENABLE}=3.3 V
Input bias current RCIN (internal current source)		I_{RCIN}		2.8			V_{RCIN} = 2 V
Mean output current for load capacity		I_{O+}	120	165	-	mA	C_L=10 nF

[1] Not subject of production test, verified by characterisation

Table 8 Static parameters

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
charging in range from 3 V (20%) to 6 V (40%)						
Peak output current turn on (single pulse)	I_{Opk+}[1]		240			R_L = 0 Ω, t_p <10 µs
Mean output current for load capacity discharging in range from 12 V (80%) to 9 V (60%)	I_{O-}	250	375	-		C_L=10 nF
Peak output current turn off (single pulse)	I_{Opk-}[1]		420			R_L = 0 Ω, t_p <10 µs
Bootstrap diode forward voltage between VCC and VB (for types with bootstrap diode only)	$V_{F,BSD}$	-	1.0	1.3	V	I_F=0.5 mA
Bootstrap diode forward current between VCC and VB (for types with bootstrap diode only)	$I_{F,BSD}$	27	51	75	mA	V_F=4 V
Bootstrap diode resistance (for types with bootstrap diode only)	R_{BSD}	24	40	60	Ω	V_{F1}=4 V, V_{F2}=5 V
RCIN low on resistance of the pull down transistor	$R_{on,RCIN}$	-	40	100		V_{RCIN}=0.5 V
FAULT low on resistance of the pull down transistor	$R_{on,FLT}$	-	45	100		V_{FAULT}=0.5 V

[1] Not subject of production test, verified by characterisation

4.6 Dynamic parameters

$V_{CC} = V_{BS} = 15$ V, $V_S = V_{SS} = V_{COM}$ unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 9 Dynamic parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
Turn-on propagation delay		t_{on}	400	530	800	ns	$V_{LIN/HIN}$ = 0 or 3.3 V
Turn-off propagation delay	6EDL04I06NC 6EDL04I06PC 6ED003L06-C2	t_{off}	360	490	760		
	6EDL04N06PC		400	530	800		
Turn-on rise time		t_r	-	60	100		$V_{LIN/HIN}$ = 0 or 3.3 V C_L = 1 nF
Turn-off fall time		t_f	-	26	45		
Shutdown propagation delay ENABLE		t_{EN}	-	780	1100		V_{EN}=0
Shutdown propagation delay ITRIP		t_{ITRIP}	400	670	1000		V_{ITRIP}=1 V
Input filter time ITRIP		$t_{ITRIPMIN}$	155	230	380		
Propagation delay ITRIP to FAULT		t_{FLT}	-	420	700		
Input filter time at LIN/HIN for turn on and off		t_{FILIN}	120	300	-		$V_{LIN/HIN}$ = 0 & 3.3 V
Input filter time EN		t_{FILEN}	300	600	-		
Fault clear time at RCIN after ITRIP-fault, (C_{RCin}=1nF)		t_{FLTCLR}	1.0	1.9	3.0	ms	$V_{LIN/HIN}$ = 0 & 3.3 V V_{ITRIP} = 0
Dead time		DT	150	310	-	ns	$V_{LIN/HIN}$ = 0 & 3.3 V
Matching delay ON, max(ton)-min(ton), ton are applicable to all 6 driver outputs		MT_{ON}	-	20	100		external dead time > 500 ns
Matching delay OFF, max(toff)-min(toff), toff are applicable to all 6 driver outputs		MT_{OFF}	-	40	100		external dead time >500 ns
Output pulse width matching. Pw_{in}-PW_{out}	6EDL04I06NC 6EDL04I06PC 6ED003L06-C2	PM		40	100		PW_{in} > 1 µs
	6EDL04N06PC			10	100		

5 Quality disclaimer

The described properties and parameters must be confirmed by specific qualification in the final system. The results of the qualification must be open to Infineon. Otherwise Infineon does not give any design release or warranty.

It is the responsibility of the customer to select the suitable set of materials and the manufacturing processes for the final system, which complies to his requirements in respect of life time.

We recommend to avoid in particular:

- during die separation - unwanted mechanical stress on the wafer, wear out of the cutting blade or any other cutter misconfiguration possibly causing cracks, chipping and/or delamination of the passivation;
- during/after die attachment – die attach delamination causing possibly unwanted high thermal resistance, unwanted mechanical stress, or reduced electrical conductivity;
- during/after die attachment – die attach voids causing possibly unwanted high thermal resistance, unwanted mechanical stress, or reduced electrical conductivity;
- during/after die attachment – unwanted ion migration possibly causing unwanted leakage or electrical modification of the device;
- during/after die attachment – unwanted ion migration causing possibly unwanted leakage or unwanted electrical modification of the device;
- during/after die attachment – unwanted increase of thermal conductivity possibly causing unwanted overheating of the device;
- during electrical interconnect, in particular wire bonding – mechanical overstress possibly causing sheared wires and/or damaged pads;
- during electrical interconnect, in particular wire bonding – lacking bond integrity, in particular non sticking interconnects on pads possibly causing unwanted misfunction of the device and/or unwanted leakages;
- during encapsulation of the device – unwanted shrink or extension of the mould compound possibly causing corrosion;
- during encapsulation of the device – unwanted ion migration causing unwanted leakage or unwanted electrical modification of the device;
- during encapsulation of the device – unsuitable mould, unsuitable moulding processes possibly causing potentially wire sweep of electrical interconnects;
- during encapsulation of the device – sharp moudl filler components possibly causing penetration of the passivation, hence unwanted environmental influences like corrosion or ion migration etc.
- during encapsulation of the device – unsuitable mould with unsuitable thermal conductivity possibly causing overheating of the device, resulting in damage of single or multiple transistors/diodes causing non functionality of the device, uncluding unwanted leakages;
- during encapsulation of the device – unwanted low creepage distances, possibly bringing about the risk of high voltage avalanche breakthroughs;
- during encapsulation of the device – unsuitable mould and/or mouldling processes possibly causing delamination, resulting in overheating, leackages, shorts, open accessible voltage carrying parts, shortend lifetime etc.
- during encapsulation of the device – unsuitable thermal behaviour of encapsulation (expansion/shrinking, state change) possibly resulting in overheating, sheared wire, openly accessible voltage carrying parts.

6 Timing diagrams

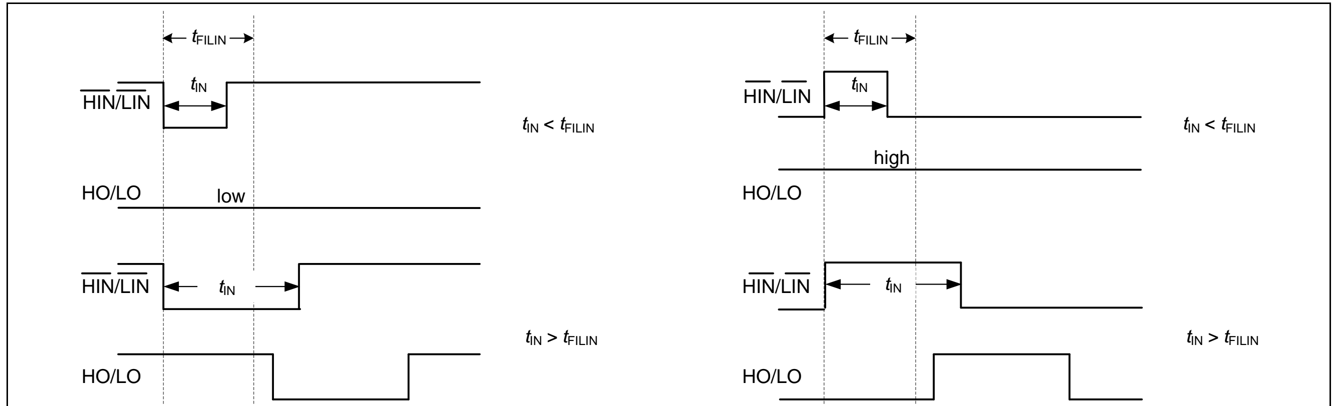


Figure 9 Timing of short pulse suppression (6EDL04I06NC, 6ED003L06-C2)

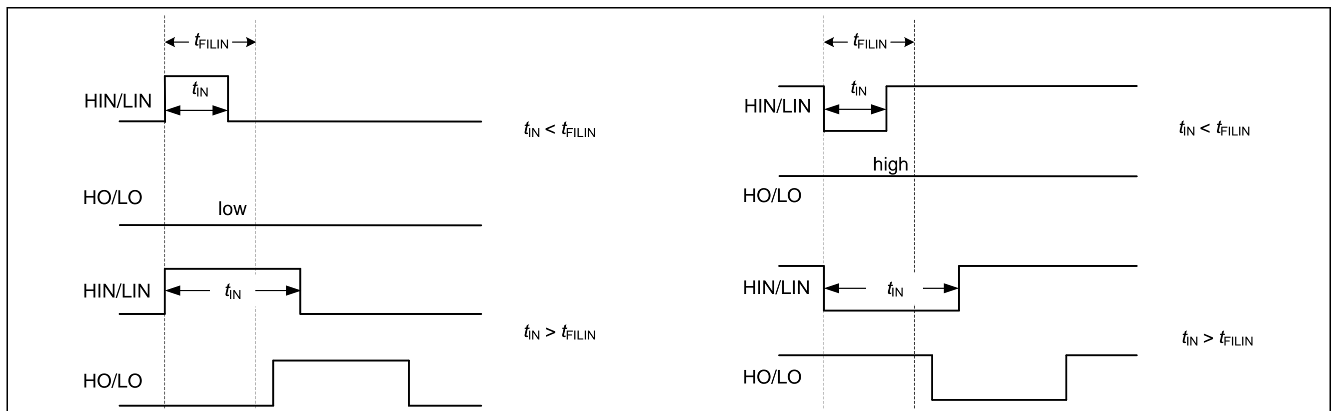


Figure 10 Timing of short pulse suppression (6EDL04I06PC, 6EDL04N06PC)

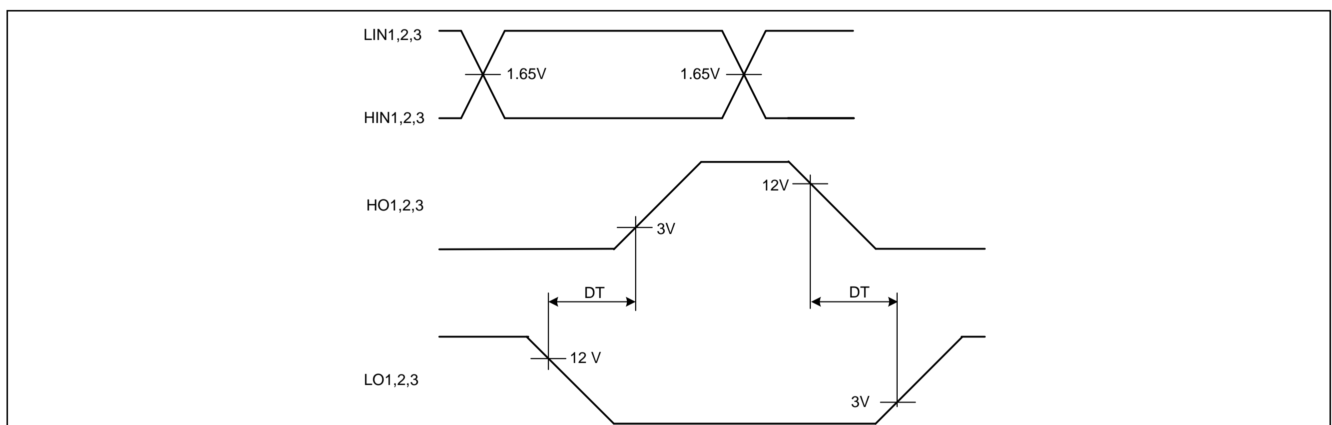


Figure 11 Timing of of internal deadtime (input logic according to Table 1)

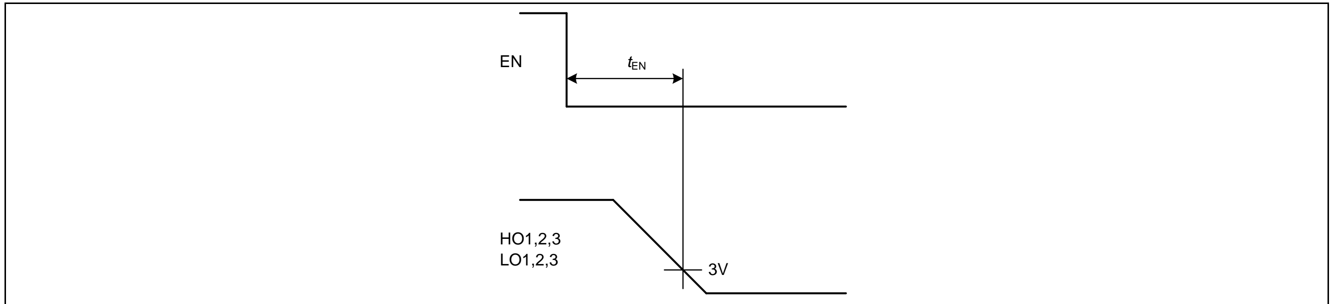


Figure 12 Enable delay time definition

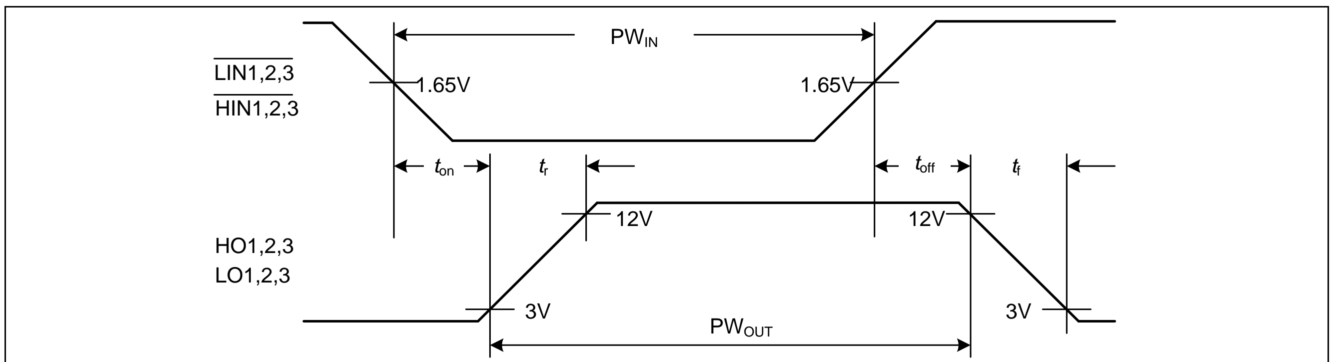


Figure 13 Input to output propagation delay times and switching times definition (6EDL04I06NC, 6ED003L06-C2)

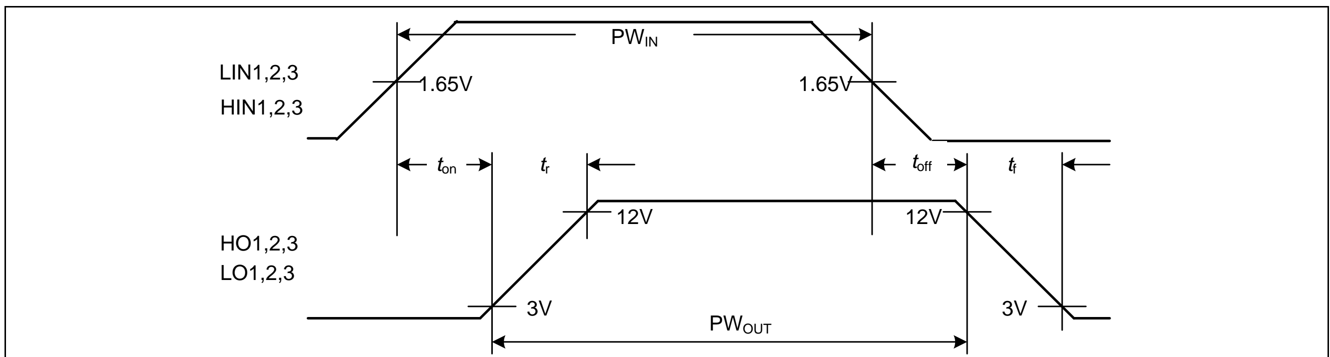


Figure 14 Input to output propagation delay times and switching times definition (6EDL04I06PC, 6EDL04N06PC)

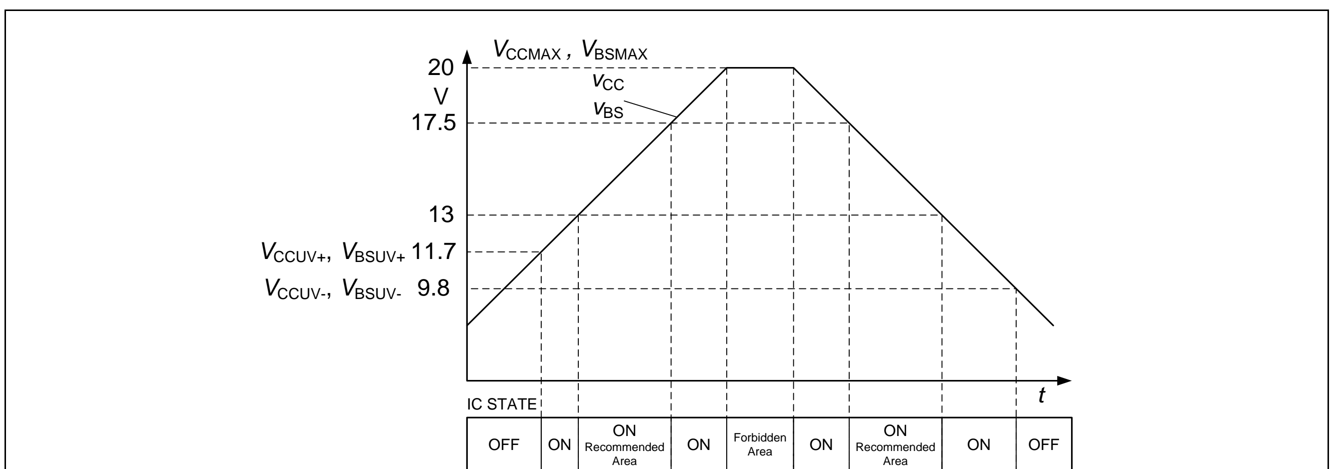


Figure 15 Operating areas (6EDL04I06NC, 6EDL04I06PC, 6ED003L06-C2)

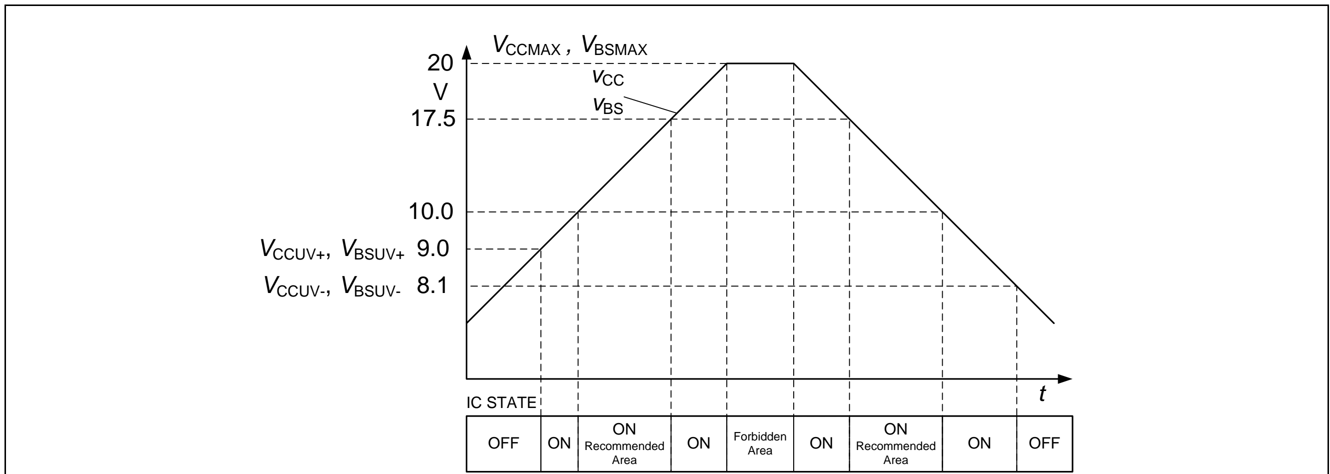


Figure 16 Operating Areas (6EDL04N06PC)

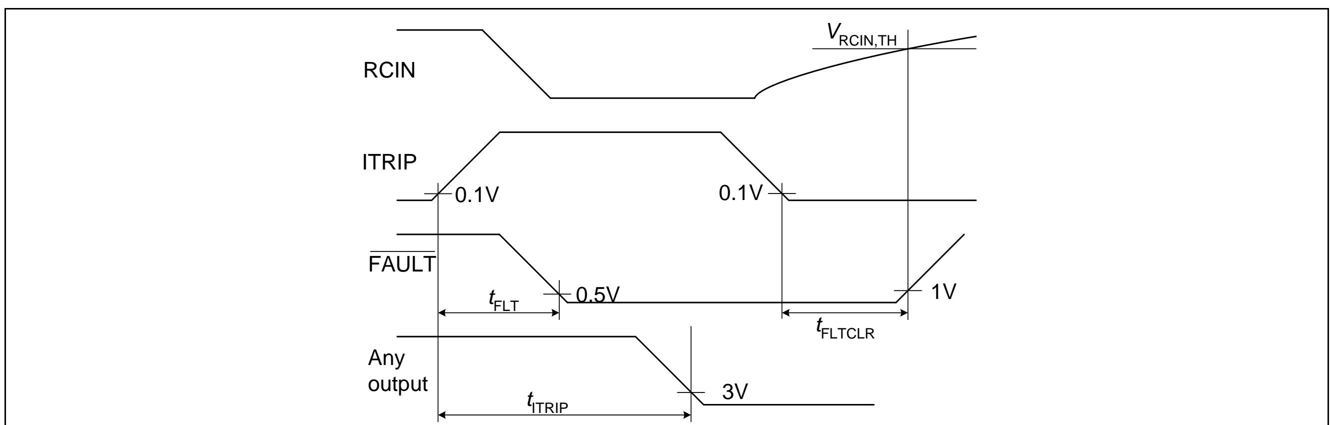


Figure 17 ITRIP-Timing

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